A detailed coupled-mode-space NEGF simulation study of source-to-drain tunnelling in gate-all-around Si nanowire MOSFETs

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In this paper we present a 3D quantum transport simulation study of source-to-drain tunnelling in gate-all-around Si nanowire transistors by using the non-equilibrium Greens function approach. The impact of the channel length, device cross-section and drain and gate applied biases on the source-to-drain tunnelling is examined in detail. The overall effect of tunnelling on the I_D-V_G characteristics is also investigated. Tunnelling in devices with channel lengths of 10 nm or less substantially enhances the off-current. This enhancement is more important at high drain biases and at larger cross-sections where the sub-threshold slope is substantially degraded. A less common effect is the increase in the on-current due to the tunnelling which contributes as much as 30% of the total on-current. This effect is almost independent of the cross-section and it depends weakly on the studied channel lengths.

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I. INTRODUCTION

Nanowire field-effect transistors (NWTs) are considered a promising alternative to the bulk MOSFET architecture, offering the possibility to extend the CMOS technology to sub-10 nm dimensions[1–5]. These devices have superior electrostatic control of the channel through the gate bias and they are not affected by the substrate leakage and channel dopant variability evident in planar devices[6–8]. Strong quantum confinement and tunnelling in NWTs calls for full-scale 3D quantum transport (QT) simulations[9]. However, these kind of simulations is usually very expensive computationally. The coupled-mode-space (CMS) approach[10–12] is one of the most efficient 3D QT simulation techniques since it greatly reduces the size of the problem when compared to real-space approaches, while, at the same time, providing sufficient accuracy. The CMS approach provides a flexible tool to understand the physics of the problem in terms of the modal decompositions and their interactions. In previous work, we have benchmarked our coupled-mode-space approach by using a fully-3D NEGF simulator for small-cross-section NWTs[13]. The CMS approach produces very close results to the fully-3D NEGF simulations in all the test cases. A detailed comparison of both simulation techniques is reported in[13]. Furthermore, the use of the CMS approach in our simulations has allowed us to extend them to large nanowire transistors. It is important to take into account that the number of modes selected for the simulation differs from case to case but, in general, more modes are required for larger cross-sections.

Tunnelling currents can be easily assessed due to the transverse-longitudinal decomposition of the Hamiltonian. Previous simulations used a non self-consistent $sp^3s^*d^5$ tight-binding model in a uniform square tunnel barrier[14] or decoupled the transport and the confinement directions assuming the electron density to be at local equilibrium in every cross-section[15], showing that source-to-drain tunnelling starts to play an important role at channel lengths below 10 nm. The source-to-drain tunnelling increases the leakage current but also significantly enhances the on-current due to the narrowing of the source-drain potential barrier at high drain voltage. This enhancement in the on-current persists at relatively long channel lengths. At the same time, a strong degradation in the sub-threshold slope is expected as the channel length of the device shrinks. Therefore, the optimal design of nanowire MOSFETs in the near-ballistic regime of operation require a careful trade-off be-

tween the detrimental tunnelling-related increase of the leakage current in the sub-threshold regime and the enhancement of the on-current at large drain bias conditions. In this paper we present a systematic study of the tunnelling as a function of channel length, cross-sectional size and bias conditions in a gate-all-around nanowire transistor. In this study we concentrate purely on the analysis of the source-to-drain tunnelling in the ballistic regime, neglecting scattering from phonons, surface roughness[16] or discrete dopants[7].

This structure of this paper is as follows: Section II describes briefly the simulation methodology and the devices that we have considered in this study. Section III, which includes the main results of this paper, presents the impact of the source-to-drain tunneling on some of the main figures of merit of the device, such as sub-threshold slope, DIBL or on-current. Finally, Section IV summarises the main conclusions of this paper.

II. SIMULATION METHODOLOGY AND DEVICE STRUCTURE

The quantum carrier transport is described using the NEGF approach, where the 3D electron density is calculated directly from the 3D mode-space Green function matrix. This calculation requires the inversion of the 3D retarded Green function G^R matrix in order to compute $G^<$, the imaginary part of which is related to the carrier density. The off-diagonal terms of $G^<$ are used to compute the electron current. The CMS method allow us to split the problem into the transverse and longitudinal spaces. The transverse space provides the cross-sectional wave functions and sub-band energies. The transport is solved in the product space of the longitudinal space with the mode space. The dimension of this space is (n_l x N), where N is the number of modes and n_l the number of nodes in the transport direction.

The Hamiltonian used in the discretization of the NEGF equations is an effective-mass Hamiltonian that folds the full crystal interaction into the electron effective masses. Due to the change in cross-section, thickness-dependent effective masses from sp^3d^5 second-neighbour-basis tight-binding calculations[17] are used in our simulations. The longitudinal and transverse effective masses are respectively 1.07 m_e and 0.30 m_e for the 2.2x2.2 nm^2 cross-section device and 0.92 m_e and 0.19 m_e for the 4.2x4.2 nm^2 cross-section device, where m_e is the electron mass. All the simulations in this work have been done at room temperature.

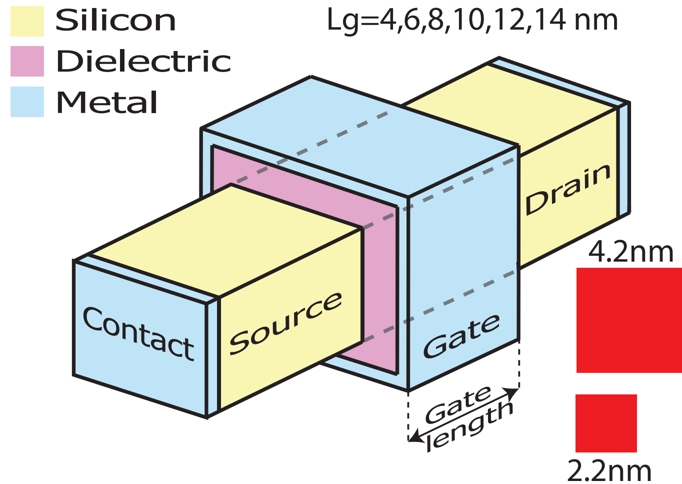

FIG. 1. Schematic view of the Si nanowire transistor.

The simulated Si NWTs, represented in Fig 1, have undoped channels, 0.8 nm SiO_2 oxide and 10 nm S/D regions doped at 10^{20} cm^{-3}. The effect of tunnelling on the on- and off-currents has been computed for two different cross-sections (2.2x2.2 nm^2 and 4.2x4.2 nm^2) and six different channel lengths (L= 4, 6, 8, 10, 12 and 14 nm). Two different drain voltages (0.05 and 0.5V) have been considered for which full I_D-V_G characteristics were simulated.

III. RESULTS AND DISCUSSION

A. Impact of Tunnelling on the Sub-threshold Slope and DIBL

Figs. 2 and 3 show the current-voltage characteristics as a function of the channel length for the NWTs with 2.2x2.2 and 4.2x4.2 nm^2 cross-sections respectively, obtained at a drain bias of 0.05 V. It is clear that the sub-threshold slope (SS) is significantly degraded as the channel length decreases. Moreover, the degradation of the SS is more significant for the larger cross-section device, which will be reflected in poorer electrostatic control when compared with the small cross-section device at equivalent channel lengths. For these two cross-sections, Table I shows the dependence of the sub-threshold slope on the channel length for the total current and its thermionic and tunnel components. As expected, the source-to-drain tunnelling is the main cause of the degradation observed in the SS. The smaller the

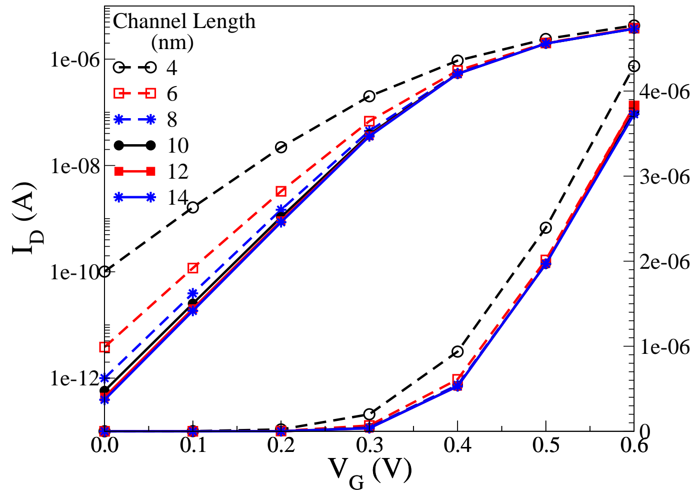

FIG. 2. I_D-V_G characteristics in linear and logarithmic scales at V_D= 0.05 V as a function of the channel length for the device with 2.2x2.2 nm^2 cross-section.

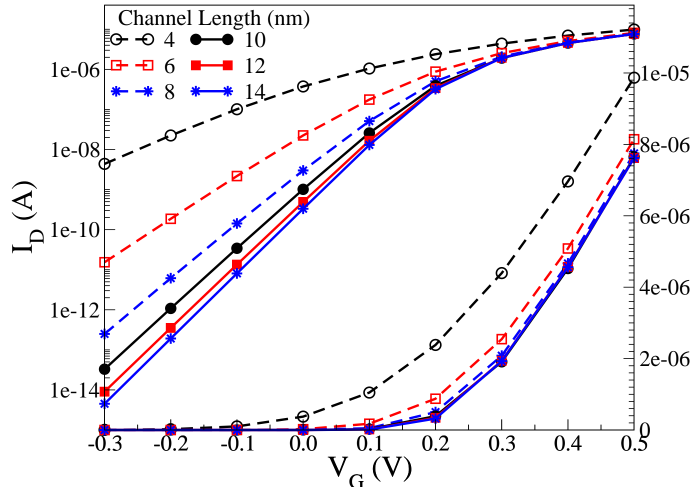

FIG. 3. I_D-V_G characteristics in linear and logarithmic scales at V_D= 0.05 V as a function of the channel length for the device with 4.2x4.2 nm^2 cross-section.

channel length of the device the more important is the tunnelling contribution to the total SS, reaching a value of 87 mV/dec at L= 4 nm for the small cross-section device. In this case the tunnel current is 87% the total current.

For the same cross-section, when the channel length is larger than 10 nm, the total SS is dominated by the thermionic contribution, remaining practically constant and close to 60mV/dec. The fraction of the tunnelling current in the total current is decreasing very rapidly with the increase in the channel length being 20% of the total at L=10 nm and 10% at L=14 nm.

TABLE I. Dependence of sub-threshold slope on the channel length for the total, thermionic and tunnel currents. The device cross-sections are 2.2x2.2 and 4.2x4.2 nm^2.

Channel Length(nm)	Sub-threshold slope (mV/dec)					
	2.2x2.2 nm^2 cross-section			*4.2x4.2 nm^2 cross-section*		
	Total	Tunnel	Thermionic	Total	Tunnel	Thermionic
4	87	91	79	192	244	166
6	75	78	70	95	101	85
10	61	65	60	72	86	68
14	60	65	60	61	63	61

The same behaviour is observed for the 4.2x4.2 nm^2 cross-section device, although for channel lengths lower than 10 nm, the degradation in the SS due to the tunnel component is much more important than the observed for the small cross-section devices, reaching a value of 192mV/dec for the L= 4 nm device. Note that for this channel length 95% of the current is due to tunnelling. At the same time the SS for channel lengths higher than 8 nm is very good, reaching 61mV/dec at L=14 nm. This value, which is very close to the ideal value for conventional MOSFETs, is almost the same as the one obtained for the smaller cross-section device.

Table II presents the drain-induced-barrier-lowering (DIBL) as a function of the channel length for the total, thermionic and tunnel currents for the two devices with different cross-sections. As expected, there is an increase in the DIBL with the reduction in the channel length. In the thermionic component this increase is only due to the decrease in the height of the potential barrier, whereas for the tunnel component the decrease in the width of the barrier also needs to be considered. This is clearly illustrated in Fig. 4, which depicts the potential distribution along the central axis of the transistor. The total DIBL is dominated by the tunnel component for channel lengths lower than 6 or 8 nm for the 2.2x2.2 or 4.2x4.2 nm^2 cross-section devices respectively. The influence of the tunnel component is decreasing with an increase in the channel length, leading to significant reductions in the total DIBL.

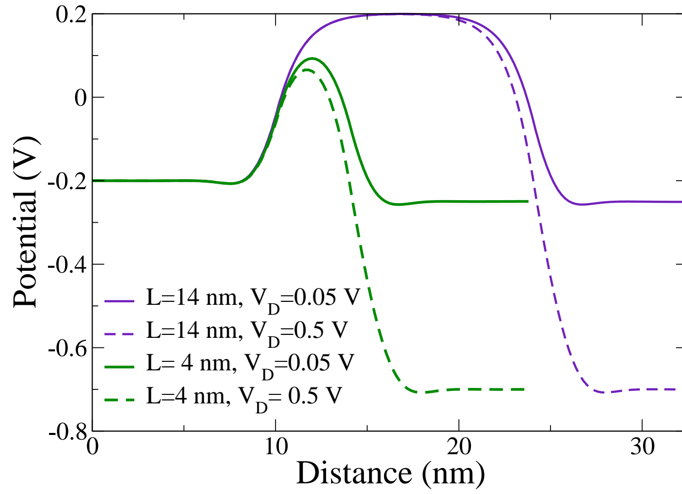

FIG. 4. Electrostatic potential as a function of the drain bias for the devices with 4 and 14 nm channel length and a cross-section of 2.2x2.2 nm^2.

TABLE II. Dependence of drain-induced barrier-lowering on the channel length for the total, thermionic and tunnel currents. The device cross-sections are 2.2x2.2 and 4.2x4.2 nm^2.

Channel Length(nm)	DIBL (mV/V)					
	2.2x2.2 nm^2 cross-section			*4.2x4.2 nm^2 cross-section*		
	Total	Tunnel	Thermionic	Total	Tunnel	Thermionic
4	55	59	39	156	161	135
6	24	30	18	83	88	58
10	7	17	5	24	44	20
14	4	9	4	9	17	8

B. Influence of the Channel Length and Applied Drain Bias

Figs. 5 and 6 show the total and the tunnelling currents as a function of the applied gate bias for both low and high drain voltages for the devices with a 2.2x2.2 nm^2 cross-section and 6 and 10 nm channel lengths respectively. Note that for the 10 nm channel length device, at a very low gate bias, the current is virtually independent of the applied drain bias. This is not the case for the shorter channel lengths transistors. This effect can be explained using

the Landauer formula[18] for the current,

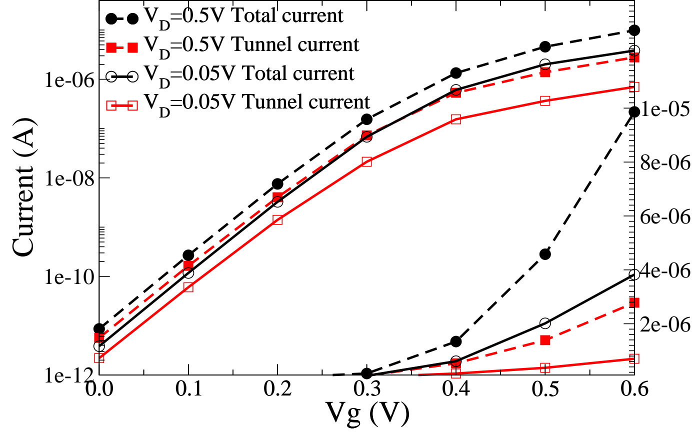

FIG. 5. I_D-V_G characteristics in linear and logarithmic scales for the total and tunnel currents at V_D= 0.05 and 0.5 V for the device with a channel length of 6 nm and a 2.2x2.2 nm^2 cross-section.

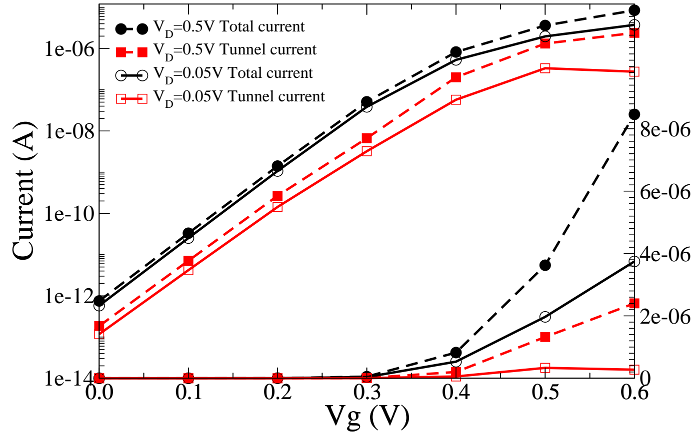

FIG. 6. I_D-V_G characteristics in linear and logarithmic scales for the total and tunnel currents at V_D= 0.05 and 0.5 V for the device with a channel length of 10 nm and a 2.2x2.2 nm^2 cross-section.

$$J = \frac{2q}{h} \int T(\varepsilon)(f_S(\varepsilon) - f_D(\varepsilon))d\varepsilon \tag{1}$$

which relates the transmission coefficient $T(\varepsilon)$ and the Fermi distributions in the S/D, $f_S(\varepsilon)/f_D(\varepsilon)$. In both bias conditions the influence of the current coming from the drain is negligible due to the small values of $f_D(\varepsilon)$ in the integral when compared to $f_S(\varepsilon)$. In the case of shorter channel lengths the tunnelling current plays an important role, due to a much

larger transmission coefficient $T(\varepsilon)$, making a large difference between high and low drain voltages.

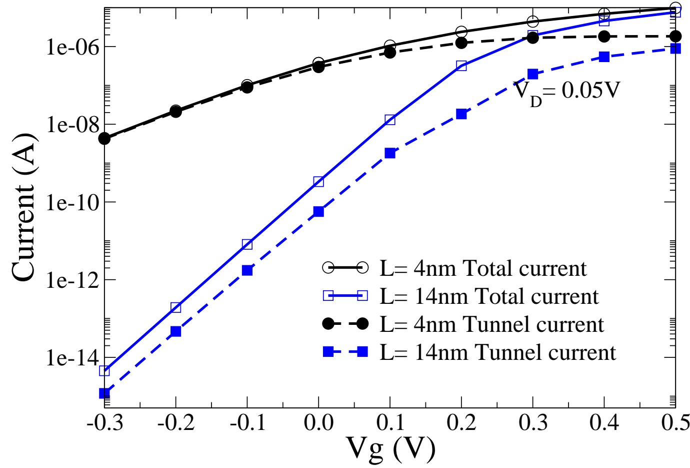

FIG. 7. I_D-V_G characteristics for the total and tunnel currents at V_D= 0.05 V for the devices with channel lengths of 4 and 14 nm and a cross-section of 4.2x4.2 nm^2.

For the larger cross-section device, a comparison of the I_D-V_G characteristics at low drain bias for the devices with L= 4 and 14 nm is presented in Fig. 7. Note the important degradation in the sub-threshold slope when the channel length is reduced to 4 nm. However, the on-current is very similar for both channel lengths.

As seen in Tables I and II, the degradation of the tunnelling current is more serious in the larger cross-section devices because of their poorer electrostatic integrity and more pronounced reduction in both the height and width of the S/D barrier with a decrease in the channel length. This effect is particularly strong at high drain bias resulting in much higher values of the SS and the DIBL.

The S/D barrier along the central axis of the channel as a function of the channel length is plotted in Figs. 8 and 9 for the 2.2x2.2 and 4.2x4.2 nm^2 cross-section devices. The applied gate and drain biases are 0.0 V and 0.05 V respectively. Both the narrowing and the reduction of the barrier due to DIBL are responsible for the increase in the off-current at shorter channel lengths. For the 4.2x4.2 nm^2 cross-section devices, there is a clear reduction in the height of the S/D barrier when the channel length is decreased. However, for the small cross-section device, the reduction in the height of the barrier is only noticeable for channel lengths lower than 10 nm. Moreover, for a particular channel length, both the height and the width of the barrier are always higher for the small cross-section devices when compared

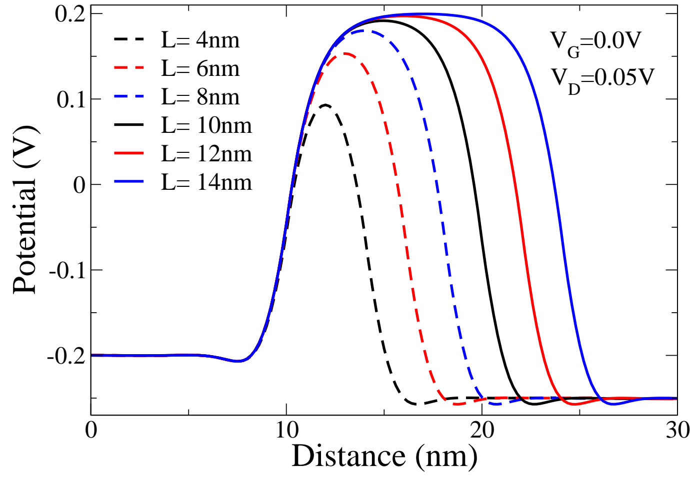

FIG. 8. Electrostatic potential as a function of the channel length for the device with a cross-section of 2.2x2.2 nm^2.

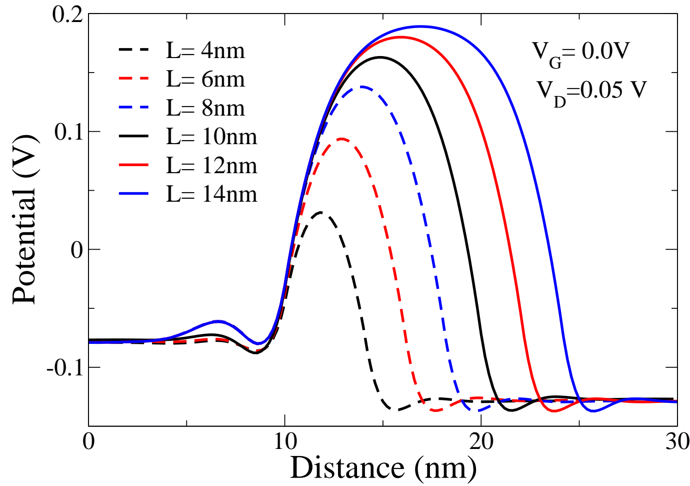

FIG. 9. Electrostatic potential as a function of the channel length for the device with a cross-section of 4.2x4.2 nm^2.

to the large cross-section ones. Therefore, the effect of the tunnelling is more important for the 4.2x4.2 nm^2 cross-section devices than for the small cross-section ones due to their worse electrostatic control.

C. Impact of the Source-to-Drain Tunnelling

Table III show the corresponding percent of tunnelling current component for the off- and on-current situations at V_D=0.05 and 0.5 V respectively for the 2.2x2.2 nm^2 cross-section device. At both low and high drain biases, the percentage of tunnelling off-current decreases with an increase in the channel length of the device. Its value is larger than the thermionic

TABLE III. Tunneling current (as a percentage of total current) as a function of the channel length at drain biases of 0.05 and 0.5 V. The device cross-sections are 2.2x2.2 and 4.2x4.2 nm^2.

Channel Length (nm)	Tunneling current (% of total current)							
	2.2x2.2 nm^2 cross-section				*4.2x4.2 nm^2 cross-section*			
	V_D=0.05V		V_D=0.5V		V_D=0.05V		V_D=0.5V	
	I_{off}	I_{on}	I_{off}	I_{on}	I_{off}	I_{on}	I_{off}	I_{on}
4	86	31	90	36	79	17	92	38
6	57	18	66	30	68	8	91	37
8	34	16	38	32	48	4	75	37
10	20	17	24	36	36	3	44	30
12	13	19	14	34	25	2	30	29
14	7	19	9	30	17	2	22	27

component for channel lengths shorter than 8 nm. For a 14 nm channel length the tunnelling off-current is reduced to less than 10% of the total current. However, the variations in the percentage of tunnelling on-current are not so dramatic, ranging between 30% of the total current for L= 4 nm and 20% for L= 14 nm at low drain bias, and slight variations are observed at high drain bias. It should be noted that in channel lengths larger than 12 and 10 nm for low and high drain bias conditions respectively the percentage tunnelling on-current is higher than the off one.

Fig. 10 plots the gate bias dependence of the S/D barrier at V_D=0.5 V for a fixed channel length of 14 nm. At low gate biases the source-to-drain barrier is flat which makes electron tunnelling difficult. At gate voltages larger than 0.3 V, the source-to-drain barrier is significantly narrower and its height decreases as we shift from source to drain. This shape of the barrier strongly favours tunnelling.

The on/off tunnelling current percentages for 4.2x4.2 nm^2 cross-section devices are also shown in Table III at low and high drain bias respectively. At low drain bias, the off-current

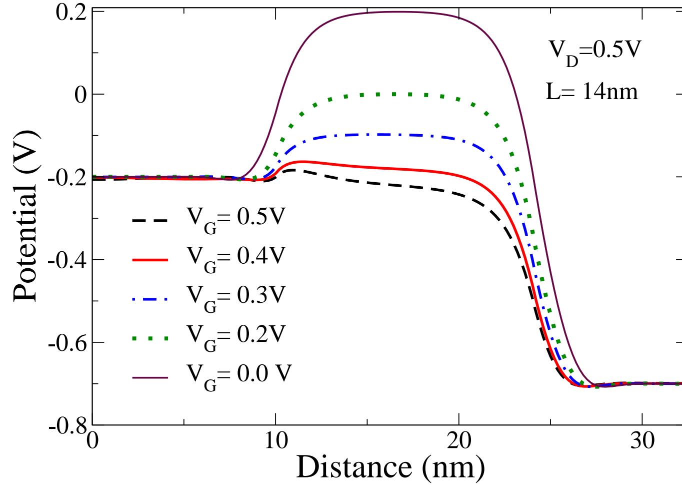

FIG. 10. Electrostatic potential as a function of the gate bias for the device with a cross-section of 2.2x2.2 nm^2.

is mostly tunnelling current for 4 and 6 nm channel length devices and 50% of the total current for 8 nm channel length device. The tunnelling off-current decreases to 20% of the total current for L = 14 nm. At high drain bias the behaviour is very similar, although in this case the tunnelling off-current is predominant up to a channel length of 8 nm, reaching approximately the 90% of the total current for channel lengths of 4 and 6 nm. The tunnelling on-current percentages are larger as compared with the corresponding low drain results.

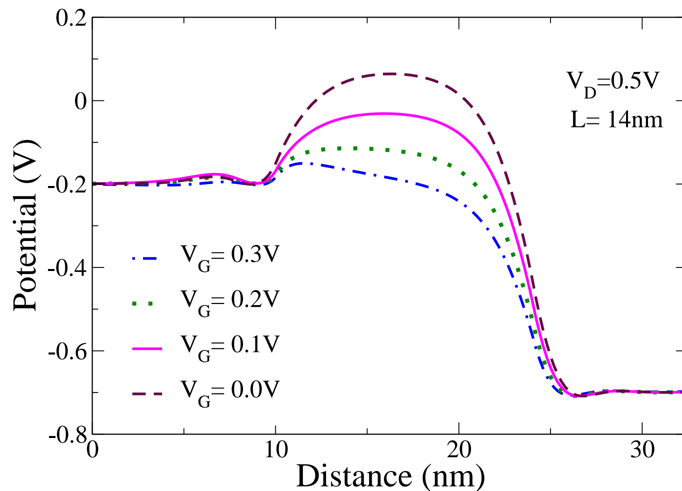

FIG. 11. Electrostatic potential as a function of the gate bias for the device with a cross-section of 4.2x4.2 nm^2.

Summarising, the percentage of tunnelling on-current spans between 15% and 3% for

low drain bias and between 35% and 25% for high drain bias. Note that at low drain bias the tunnelling on-current contribution is lower when compared to the small cross-section devices. This is a consequence of the poorer electrostatic control of the barrier in the large cross-section device compared to the small cross-section one. However, at high drain bias the tunnelling on-current shows similar effects when compared to the small cross-section case. This is a consequence of the narrowing of the barrier when the gate bias is increased. This narrowing can be observed in Fig. 11, which shows the S/D barrier along the channel as a function of the applied gate bias for the large cross-section device, where the channel length considered is 14 nm and the drain bias 0.5 V.

IV. CONCLUSIONS

We have studied the effect of the source-to-drain tunnelling on the I_D-V_G characteristics of a Si nanowire transistor. The NEGF formalism in the coupled-mode approximation has been used to calculate the current and to analyse the tunnelling component contribution. The impact of tunnelling on both on- and off-currents has been analysed in detail for two different device cross-sections and six different channel lengths. Results show a noticeable degradation in the sub-threshold slope and a corresponding increase in the off-current due to the impact of the source-to-drain tunnelling for devices with channel lengths below 10 nm. This degradation is more dramatic for devices with larger cross-sections. Tunnelling can also be particularly significant at high drain and gate voltage (on-current) conditions for longer channel lengths. The tunnelling component of the on-current is approximately 30% at high drain bias and it is relatively independent of the channel length. As a general conclusion, the tunnelling effect under 10 nm can significantly increase the leakage. However, for all studied channel lengths it provides a beneficial increase in the on-current.

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