0.6-V-V_{IN} 7.0-nA-I_Q 0.75-mA-I_L CMOS Capacitor-Less LDO for Low-Voltage Micro-Energy-Harvested Supplies

Óscar Pereira-Rial, Paula López, *Member, IEEE*, and Juan M. Carrillo

***Abstract*— A capacitor-less (CL) low-dropout (LDO) regulator suitable to be incorporated in an on-chip system with low-voltage micro-energy-harvested supply, is proposed in this contribution. The differential input stage of the error amplifier includes bulk-driven MOS transistors, thus providing the LDO with an output voltage range that extends from the negative rail up to a level very close to the input voltage without the need of using a resistive feedback network. The circuit parameters relying on the feedback factor, β, are maximized thanks to the use of a unitary value for this parameter. The CL-LDO has been designed and fabricated in standard 180-nm CMOS technology and optimized to operate with an input voltage equal to 0.6 V and a reference level of 0.5 V. The experimental characterization of the fabricated prototypes shows that, under these operating conditions, the LDO is able to deliver a load current above 0.75 mA with a total quiescent current of only 7.0 nA. Furthermore, the proposed voltage regulator is able to operate from input voltages as low as 0.4 V, delivering in this case a maximum load current of 30 μA.**

***Index Terms*— Bulk-driven MOS, capacitor-less LDO, energy harvesting, low-power, low-voltage.**

I. Introduction

THE power management unit (PMU) of an integrated circuit (IC) must be efficiently designed to increase the autonomy of portable systems-on-chip. This aspect is especially important in solutions intended for internet-of-things (IoT) [1], wireless remote sensing [2], biomedical applications [3] or wearable devices [4], in which different functions may remain in the stand-by mode most of the time and are activated when needed during a short time slot. Under these circumstances, a low quiescent current leads to an increase of the battery life, whereas a high load current should be delivered rapidly and during a very short time lapse when required. Switched regulators present a very high efficiency and allow programmability of the output voltage. Nevertheless, the inherent ripple superimposed to the generated voltage results critical for high-performance analog front-ends [5]. Therefore, a low-dropout (LDO) regulator may be used to generate the required spurious-free and stable supply voltage [5]–[45]. Besides, capacitor-less (CL) LDOs result very compact and suitable to reduce the cost of the prototype, as the internal compensation of its frequency response allows avoiding the use of bulky off-chip load capacitors [23].

The drastic variations suffered by the load current when different parts of an IC are switched on and off require a very fast response of the LDO, so that it can supply currents from the nA to the mA range and vice-versa nearly instantaneously. For this reason, large biasing currents should be available in the LDO during the transitions of the load current, in order to speed up its time response, whereas the stand-by operating mode should be accompanied by a very reduced current consumption, i.e., a very low quiescent current, I_Q. On the other hand, the efficiency of an LDO is increased when the difference between the input voltage, V_{IN}, and the output voltage, V_{OUT}, is reduced. Furthermore, in case micro energy harvesting is used to supply the IC, a power management integrated circuit (PMIC) including a switching DC-DC power converter and an LDO can be considered. In this case, biasing the LDO with a low V_{IN} would allow reducing the number of stages of the capacitive DC-DC converter, with the consequent decrease in silicon area and increase of the efficiency.

The conventional structure of a CL-LDO is illustrated in Fig. 1a and consists of an error amplifier (EA), a pass transistor, M_P, and a feedback network with a gain equal to β, known as feedback factor. The value of V_{OUT}, is a function of a reference voltage, V_{REF}, and may be expressed as:

$$V_{OUT} = V_{REF} \cdot \frac{A_{EA}}{1 + \beta A_{EA}} \approx V_{REF} \cdot \frac{1}{\beta} \tag{1}$$

where A_{EA} is the DC gain of the error amplifier. As inferred from (1), the output voltage may be set with the help of the feedback factor and its DC value does not rely on the input voltage provided that the pass transistor operates in saturation. The source-to-drain voltage of M_P, $V_{SD} = V_{IN} - V_{OUT}$, is known as dropout voltage and may be reduced by

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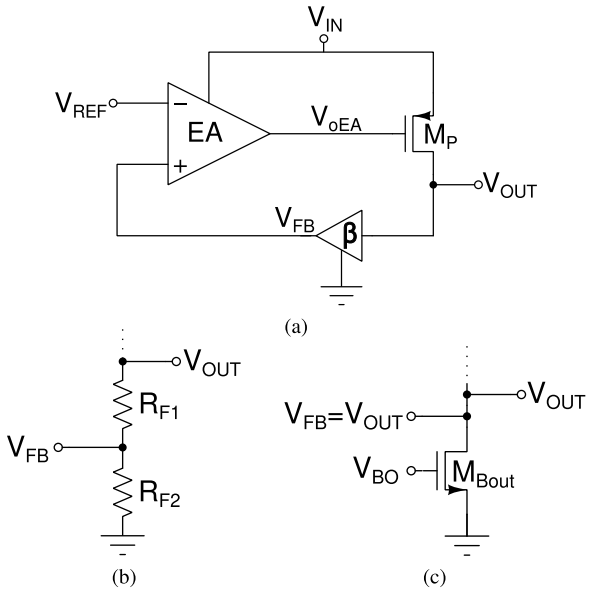

Fig. 1. CL-LDO: (a) general block diagram, (b) resistive feedback network and (c) unitary feedback configuration.

sizing this device with a very large aspect ratio, which also provides a high drive capability. The feedback network may be implemented by following the approaches illustrated in Figs. 1b and 1c, for which the feedback loop transfer function is

$$LG(s) = \beta \cdot A_{EA}(s) \cdot A_p(s) \tag{2}$$

where $A_p(s) = g_{m,M_P} \cdot (r_{o,M_P} || r_{o,M_{Bout}} || R_L || C_{out})$ is the intrinsic gain of the pass stage, g_{m,M_P} and r_{o,M_P} are the transconductance and output resistance of transistor M_P, respectively, and $r_{o,M_{Bout}}$, R_L, and C_{out} are the output resistance of transistor M_{Bout}, the load resistance, and the output capacitance, respectively. In the approach in Fig. 1b [7], [8], [12], [15], [20], [22], [35], the feedback is established with the help of two resistors, leading to a feedback factor $\beta = R_{F2}/(R_{F1} + R_{F2}) < 1$. In the solution in Fig. 1c [9], [31], [37], [43], $\beta = 1$ and, according to (1), the output voltage of the LDO is nominally equal to the reference voltage.

Unlike the DC behavior, the response of the AC output voltage, v_{out}, is affected by undesired signals at the input voltage, v_{in}, according to the expression [10]:

$$v_{out} = \left[\frac{1 - A_{oEA}}{\beta A_{EA}} + \frac{1}{A_p} \cdot \frac{1}{\beta A_{EA}} \right] v_{in} \tag{3}$$

where A_{oEA} is the gain from the supply to the output of the error amplifier, i.e., v_{oEA}/v_{in}. In view of (3), it becomes evident that the effect of the power supply on the output voltage of the LDO may be minimized by maximizing the value of β. Nevertheless, in the limit case in which $\beta = 1$, i.e., when an unitary feedback is established, the maximum achievable value of V_{OUT} could be limited by the input common-mode (CM) voltage range of the EA.

On the other hand, the on-chip implementation of the resistors required in the feedback configuration in Fig. 1b supposes a challenge in an ultra-low-power LDO, in which quiescent currents in the nA range are required at the pass branch. A common solution to overcome this drawback is to implement the resistive divider by means of a network including active devices, such as diode-connected MOS transistors [21], [39], [41]. In any case, the quiescent current flowing through the output branch depends on the value of the output voltage selected. Furthermore, the low-to-high transition of the load current can be very fast, provided that the pass transistor is properly driven, whereas the high-to-low transition of the load current may be slowed down by the feedback network. On the other hand, the use of a resistive feedback network leads to lower gain and bandwidth of the feedback loop inherent in the LDO [23], which becomes evident from (2). Finally, it is worth to point out that the output noise of the LDO increases as the value of the feedback factor is reduced.

Despite the apparent limitations of using a feedback network as the one illustrated in Fig. 1b, a feedback factor lower than unity relaxes the input CM voltage range requirements of the EA, allowing V_{OUT} to range nearly from rail to rail with only a part of the voltage range available for V_{REF}. Indeed, the use of the feedback structure illustrated in Fig. 1c leads to nominally higher power supply rejection (PSR) and lower output noise, and offers the possibility to provide the output branch with a class-AB biasing, but a wide programmability of V_{OUT} must be accompanied by an extended input CM voltage range of the EA.

The use of bulk-driven (BD) MOS transistors [46]–[48] at the input stage of the EA allows operation under lower supply voltages, as well as an increase of its input voltage range and, consequently, of the output voltage of the LDO. Indeed, in a BD transistor the bias and signal components of the input voltage are applied to the gate and the bulk terminal, respectively, thus leading to a reduction of the value of V_{IN} required for proper operation. As a consequence, using a feedback factor $\beta = 1$ in the LDO, as shown in Fig. 1c, becomes compatible with setting V_{OUT} at any level between ground and very close to V_{IN}.

In this contribution the design of a low-voltage ultra-low-power CL-LDO is presented. The voltage regulator has a quiescent current as low as 7.0 nA and can deliver a load current of approximately 0.75 mA while operating with V_{IN} 0.6 V. Besides, the LDO is able to operate with an input voltage as low as 0.4 V. To the best of our knowledge, the proposed LDO uses the lowest supply voltage ever reported in the literature [16], [37] without using any boosting of the input voltage [40], while featuring a significant $I_{L,max}/I_Q$ ratio. The rest of the manuscript has been organized as follows. In Section II a comparison between the use of a gate-driven (GD) and a BD error amplifier is established. Section III presents the proposed LDO, including the main design considerations, and experimental results are provided in Section IV. Finally, conclusions are drawn in Section V.

II. BD vs GD Error Amplifier

The error amplifier of an LDO that follows the structure illustrated in Fig. 1a typically includes a differential input

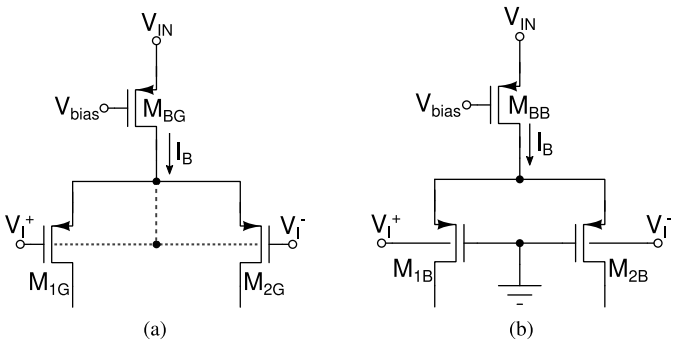

Fig. 2. PMOS differential pair: (a) gate-driven and (b) bulk-driven.

stage as the one depicted in Fig. 2a. The input CM voltage range of the GD PMOS approach shown may be expressed as

$$V_{GND} \leq V_{I_{EA},CM(GD)} \leq V_{IN} - V_{SG,M_{1G-2G}} - |V_{DSat,M_{BG}}| \tag{4}$$

where $V_{SG,M_{1G-2G}}$ and $V_{DSat,M_{BG}}$ are the source-to-gate voltage of transistors M_{1G} and M_{2G} and the source-to-drain saturation voltage of device M_{BG}, respectively. The inherent limitation of $V_{I_{EA},CM}$ close to V_{IN} may be overcome by properly selecting the feedback network in Fig. 1b. Conversely, if the feedback configuration in Fig. 1c is intended to be used, to take advantage of the inherent advantages previously enumerated, the limitation of the input CM voltage range of the EA close to V_{IN} will constrain the output voltage range of the LDO in this region. Besides, the minimum supply voltage imposed on the LDO by the error amplifier is

$$V_{IN,min(GD)} \geq V_{REF} + V_{SG,M_{1G-2G}} + |V_{DSat,M_{BG}}| \tag{5}$$

The minimum supply voltage required for proper operation of the EA, and hence of the LDO, relies on the value of V_{REF} and is also related to the limitation of the PMOS input stage to operate close to V_{IN} described in (4). These constraints cannot be alleviated by the feedback network, as they are inherent to the GD implementation of the input stage of the EA and to the non-inverting nature of the feedback loop. At this point, it is worth to point out that using a GD NMOS differential pair in the EA would lead to a limitation of the output voltage range of the LDO in the voltage region close to ground.

The restrictions of a GD PMOS differential pair regarding the input CM voltage range and the minimum V_{IN} may be overcome by using the BD PMOS differential pair illustrated in Fig. 2b. In a BD transistor the bias voltage required to turn the device on, applied at the gate, and the signal voltage, applied at the bulk, are decoupled. For this reason, the input CM voltage range of a BD differential pair becomes

$$V_{GND} \leq V_{I_{EA},CM(BD)} \leq V_{IN} \tag{6}$$

whereas the minimum supply voltage of an EA with a BD input stage may be written as

$$V_{IN,min(BD)} \geq V_{SG,M_{1B-2B}} + |V_{DSat,M_{BB}}| \tag{7}$$

where $V_{SG,M_{1B-2B}}$ and $V_{DSat,M_{BB}}$ are the source-to-gate voltage of transistors M_{1B-2B} and the source-to-drain saturation voltage of device M_{BB}, respectively. Indeed, as the reference voltage is applied to the bulk terminal of one of the input devices, the input CM voltage range may be swept from rail-to-rail [46], as inferred from (6). Besides, the value of the minimum supply voltage that can be used relies on the path from the gate terminal of the input devices, both connected to ground as observed in Fig. 2b, to V_{IN}. Therefore, the limitation introduced by V_{REF} in (5) for a GD PMOS differential pair is eliminated from (7) for the BD counterpart.

Despite the advantages of the BD technique indicated above, there are also limitations associated to this approach. First of all, the bulk transconductance, g_{mb}, is smaller as compared to the gate transconductance, g_m, depending the attenuation factor on the transistor inversion level and being their ratio $g_{mb}/g_m \approx 1/3$ in the CMOS technology selected and with the current level used in this work. The reduction of the transconductance directly affects the maximum achievable frequency range and increases the value of input referred magnitudes, such as the offset voltage and the noise, due to the lower intrinsic gain of a BD device as compared to its GD counterpart [48]. Besides, in an *n*-well technology the BD devices must be PMOS type, in order to be able to place each transistor in its own tub. Thus, the active region of the source terminal, *p*-type, and the bulk terminal, *n*-type, form a parasitic *pn* junction, which is forward biased when the bulk voltage becomes lower than the source voltage. Even though the risk of latch-up is practically eliminated by properly editing the layout of the BD transistors, the current flowing through the bulk terminal must be reduced to a minimum in order to avoid loading effects on preceding stages. Even though these restrictions could seem limiting at first sight, the use of BD transistors in the design of a differential input stage leads to input rail-to-rail operation [48] and allows to noticeably reduce the value of the input voltage of the LDO as compared to the case of a GD input section.

III. Low-Voltage BD CL-LDO

With the goal of obtaining a low-voltage ultra-low-power voltage regulator, a PMOS BD differential input stage has been used in the error amplifier. The overall circuit schematic of the proposed CL-LDO is illustrated in Fig. 3. As observed, the EA consists of two gain stages. The first section includes a BD input differential pair, transistors M_{1B}-M_{2B} and M_{BP}, and a folded-cascode summing stage, devices M_{C1}-M_{C8}, with on-chip generation of the corresponding biasing voltages V_{CN}, V_{BN} and V_{CP}. Besides, the second gain stage, consisting of transistors M_{S1} to M_{S4}, is a non-inverting section that allows providing stability to the LDO in a straightforward manner. Indeed, the nested Miller frequency compensation strategy was followed by connecting the compensation capacitors C_{C1} and C_{C2} between V_{OUT} and V_{oEA} and V_{OUT} and V_{o1}, respectively. Furthermore, the pass branch includes the pass transistor, M_P, which is biased by a PMOS transistor, M_{Bout}, with its gate connected to V_{REF} and the source connected to V_{OUT}. The goal of this configuration is twofold. In the

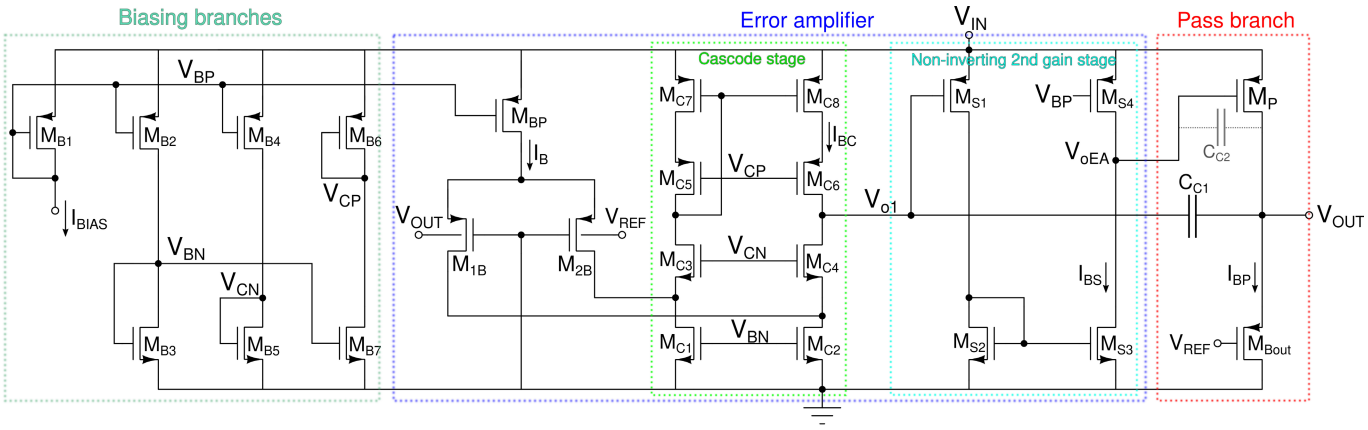

Fig. 3. Proposed low-voltage CL-LDO with bulk-driven differential pair in the error amplifier.

quiescent operation, the values of the gate and source voltages applied to transistor M_{Bout} are very close, due to the virtual ground in the EA. Thus, this device is biased in the deep subthreshold region, providing a biasing current that may be determined by [49]

$$I_{D,M_{Bout}} = I_{BP} = I_s \cdot e^{\left(\frac{-V_{th}}{nV_T}\right)} \tag{8}$$

where I_s is the characteristic current, n is the subthreshold slope factor and V_T is the thermal potential. In the case of a sudden change in the load current, in particular in the high-to-low transition, the value of V_{OUT} will increase, causing a higher source-to-gate voltage difference in transistor M_{Bout} that speeds up the discharge of the output node. On the other hand, when the low-to-high load current transition takes place, the high drive capability of the pass transistor M_P allows rapidly charging the output node provided that it is properly driven by the preceding stage.

The minimum input voltage that may be used for the LDO shown in Fig. 3 is constrained by the operation in saturation of all the transistors in the folded-cascode summing stage. The very low level of the biasing current required for ultra-low power consumption forces all the devices in the cascode section to operate in the subthreshold region, where $V_{DS,min} \approx 4V_T$. Thus, the minimum value of V_{IN} is expected to be around 0.4 V. Next, the most important design considerations associated to the use of BD transistors at the input stage of the EA of a CL-LDO are discussed.

A. Stability

The use of a two-stage EA leads to a three-stage configuration for the overall CL-LDO. The presence of three gain stages increases the low frequency accuracy of the LDO, as well as boosts the DC value of the PSR. Nevertheless, careful frequency compensation must be carried out. Two compensation capacitors, C_{C1} and C_{C2} in Fig. 3, are required, being connected each between nodes with a phase inversion, reason why the second gain stage has to be non-inverting. The transfer function of the open-loop gain around the LDO may be expressed as [50]:

$$LG(s) = \frac{A_{EA}A_p\left(1 - s\frac{C_{C2}}{g_{m,M_P}} - s^2\frac{C_{C1}C_{C2}}{g_{m,M_{S3}}g_{m,M_P}}\right)}{\left(1 + \frac{s}{\omega_{-3dB}}\right)\left[1 + s\frac{C_{C2}\left(g_{m,M_P} - g_{m,M_{S3}}\right)}{g_{m,M_{S3}}g_{m,M_P}} + s^2\frac{C_L C_{C2}}{g_{m,M_{S3}}g_{m,M_P}}\right]} \tag{9}$$

where

$$\omega_{-3dB} = \frac{g_{o1}g_{o2}g_{o3}}{C_{C1}g_{m,M_{S3}}g_{m,M_P}} \tag{10}$$

is the frequency of the dominant pole and g_{oi}, with $i = 1$ to 3, represents the output conductance of the i-th stage. Equation (9) shows that there are three poles and two zeros in the signal path. The minimum load current that may be achieved is determined by the value of g_{m,M_P} and, hence, by the position of the poles and zeros with respect to the unity gain frequency so that a sufficiently high phase margin may be obtained. For an optimally designed LDO, stability must be ensured even in the case of a light load current, that is, when the load current is equal to zero. Taking into account that the total DC gain of the loop is

$$LG = A_{EA}A_p = \frac{g_{mb,M_{1B-2B}}g_{m,M_{S3}}g_{m,M_P}}{g_{o1}g_{o2}g_{o3}} \tag{11}$$

the loop gain-bandwidth product is easily obtained as

$$LG_{BW} = LG \cdot \omega_{-3dB} = \frac{g_{mb,M_{1B-2B}}}{C_{C1}} \tag{12}$$

The bandwidth of the LDO's feedback loop is theoretically reduced by the inherently lower value of the bulk transconductance, which appears in the numerator of (12), as compared to the gate transconductance. Nevertheless, the impact of g_{mb} on the reduction of the LB_{BW} is not so evident as in a three-stage loop the maximum value of the input transconductance is limited by the position of the secondary poles. Besides, it is worth to point out that the expression of the LG_{BW} in (12) corresponds to the particular case for $\beta = 1$, which maximizes the bandwidth of the feedback loop. Indeed, in the general case, the equation of the LG_{BW} would contain the feedback factor multiplying the term in the right side of (12) [see (2)],

thus reducing the value of the LG_{BW} for the cases in which a resistive feedback is used [$\beta = R_{F2}/(R_{F1} + R_{F2}) < 1$].

B. PSR and LS

The PSR indicates the capability of the LDO to reject spurious signals in the supply voltage, so that the output voltage generated may remain as constant as possible. The line sensitivity (LS), is closely related to the PSR at low frequencies. Thus, from (3) these two parameters particularized to the proposed LDO may be written as

$$\begin{aligned} LS &\approx PSR(s=0) \\ &= \frac{(1 - A_{oEA}) \cdot g_{o1}g_{o2}}{g_{mb,M_{1B-2B}}g_{m,M_{S3}}} + \frac{g_{o1}g_{o2}g_{o3}}{g_{mb,M_{1B-2B}}g_{m,M_{S3}}g_{m,M_P}} \end{aligned} \quad (13)$$

The fact of having a bulk transconductance in the denominator of both terms in equation (13) apparently degrades the value of the supply rejection at low frequencies. Nevertheless, the PSR of the proposed approach is increased due to the adoption of an unitary feedback loop, i.e., $\beta = 1$.

C. Load Regulation

The load regulation (LR) measures the variation of the output voltage for a change in the load current. The LR is associated to the DC closed-loop output resistance of the LDO [23], which can be expressed as:

$$R_{out,cl} = \frac{R_{out}}{1 + \beta A_{EA} A_p} \quad (14)$$

Considering that $A_p = g_{m,M_P} \cdot R_{out}$ and that $\beta = 1$ for the LDO in Fig. 3, the expression in (14) may be particularized to the case of the proposed LDO as

$$R_{out,cl} \approx \frac{g_{o1}g_{o2}}{g_{mb,M_{1B-2B}}g_{m,MS3}g_{m,MP}} \quad (15)$$

On the one hand, the value of $R_{out,cl}$, and consequently of the LR, is minimized thanks to the maximization of the value of β. On the other hand, the use of BD transistors in the EA reduces its DC gain as compared to the case of a GD counterpart, thus increasing the value of the output resistance.

D. Transient Response

The output voltage of an LDO may vary due to sudden changes in the input voltage and the load current. These situations are respectively known as line transient and load transient responses. In both cases, the analysis of the responses is not straightforward, specially taking into account that the pass transistor, M_P, could operate in different regions for different load conditions. Regarding the line transient, an improvement of the PSR usually results in a higher and faster rejection to large-signal changes at the input voltage. As for the load transient, the time response of the output voltage may be limited by the response of the EA or by the behavior of the pass branch. Indeed, when a low-to-high transition in the load current takes place, the high drive capability of the pass transistor allows providing very rapidly a considerably high current to the load. In this case, the slew-rate of the EA must be optimized, so that the pass transistor may be properly driven. Conversely, in the case of a high-to-low transition of I_L the feedback network, transistor M_{Bout} in our case, is the responsible of the discharge of the output node. For this reason, the configuration described above, which leads to a very small quiescent current and a much higher current during the indicated current load transition, has been adopted.

E. Noise

The noise in an LDO includes the thermal and the flicker contribution of all the active devices. The expression of the power spectral density of the output noise of the proposed LDO may be written as follows

$$v^2_{N,out}(f) = v^2_{N,ref}(f) + v^2_{N,EA}(f) + \frac{v^2_{N,pass}(f)}{A^2_{EA}(f)} \quad (16)$$

As observed in (16), the main contributions to the output noise of the LDO are the output noise of the voltage reference and the input referred noise of the EA, whereas the noise contribution of the pass branch is negligible as it is divided by the gain of the error amplifier. Besides, it is worth to point out that the selected feedback configuration leads to a twofold reduction of the overall noise contribution. On the one hand, no feedback resistors are used and, hence, their corresponding noise contribution is avoided. On the other hand, the three noise contributions in (16) are implicitly divided by the feedback factor, which does not appear in the equation because in our case $\beta = 1$. Therefore, a value of $\beta < 1$ would lead to an increase of the total output noise. Regarding the noise contribution of the voltage reference, it may be reduced by placing a low-pass filter at the output of this circuit section. As a consequence, the main source of noise of the LDO is due to the EA. At this point, it must be indicated that the input referred noise of the proposed EA is boosted due to the presence of BD transistors, due to their inherently lower effective transconductance g_{mb} [48].

It may be concluded from previous analyses that the penalties associated to the use of BD transistors at the input stage of the EA are partially counteracted by the use of an unitary-gain feedback configuration. Indeed, taking into account that a typical value of β when a resistive feedback is established is 1/2 ($R_{F1} = R_{F2}$) and that the attenuation factor due to the use of BD transistors was indicated to be in our case $g_{mb}/g_m \approx 1/3$, both effects approximately cancel each other. In return, the use of BD transistors allows reducing the input voltage of the LDO down to a limit that may not be achieved with the use of a conventional GD EA.

IV. Experimental Results

The CL-LDO with a BD differential input stage in the error amplifier, illustrated in Fig. 3, has been designed and fabricated in 180 nm standard CMOS technology. A microphotograph of the chip is shown in Fig. 4, where the corresponding layout has also been included in order to provide the details hidden by pasivation layers implanted during the fabrication process. The circuit was optimized to operate with a nominal supply voltage $V_{IN} = 0.6$ V, $V_{REF} = 0.5$ V and

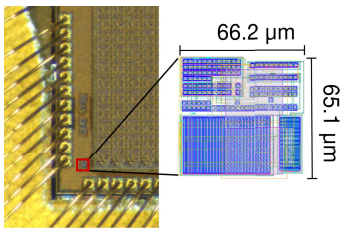

Fig. 4. Chip photography and detailed layout of the LDO.

TABLE I
SIZE OF THE MAIN DEVICES IN THE PROPOSED LDO

Device	Dimensions (μm/μm)
M_{1B},M_{2B},M_{C3},M_{C4},M_{C5},M_{C6}	20/2
M_{C1},M_{C2},M_{C7},M_{C8},M_{S1},M_{S2}, M_{S3},M_{S4}	12/2
M_P	900/1
M_{BOUT}	400/0.18
C_{C1} (MiM capacitor)	$2 \times 25/30$

$I_L = 500$ μA, even though the prototypes are able to operate with V_{IN} ranging from 0.4 V ($I_{L,max} = 30$ μA) up to 1.8 V ($I_{L,max} = 12$ mA). An external DC current of 1 nA was used to internally generate the biasing currents for all the stages of the LDO, with values $I_B = I_{BC} = I_{BS} = 1$ nA and $I_{BP} = 850$ pA, for the input differential pair, cascode stage, non-inverting section, and pass branch, respectively, even though the last value relies on the level of V_{OUT}. The sizes of the main devices in the LDO in Fig. 3 are reported in Table I. Unless different conditions are specifically stated, the experimental results indicated next have been determined from measurements over 13 samples of the silicon prototype. The experimental setup used included a Keithley 6487 picoammeter, a Keithley 2450 SMU, a National Instruments USB-6341 DAQ, and a Tektronix MDO4034C oscilloscope.

The frequency compensation passive network, consisting of capacitors C_{C1} and C_{C2} in Fig. 3, was implemented with MIM capacitors using values that ensure stability for a load capacitance of 10 pF. In fact, only capacitor $C_{C1} = 3$ pF was required to be a physical device, as the low value required for the other capacitor, $C_{C2} = 470$ fF, allowed it to be built by taking advantage of the drain-to-gate parasitic capacitance of the pass transistor M_P, $C_{dg,MP}$. In these conditions, the feedback loop in the LDO has a unity gain frequency of 144 Hz and shows a phase margin of around 78° for a load current equal to zero, that is, in the worst stability case.

The experimental output voltage, V_{OUT}, and quiescent current, I_Q, of the LDO biased with the current levels indicated previously, were determined to be equal to 517.0±9.6 mV and 6.99±0.60 nA, respectively. Besides, the experimental distributions of V_{OUT} and I_Q for the 13 samples of the circuit are shown in Fig. 5. On the one hand, the quiescent value of V_{OUT} was measured with a load current of 1 μA and the variations around the mean value are mainly attributed to the offset voltage and finite gain of the error amplifier. On the other hand, the value reported for I_Q includes the current consumption of the biasing section illustrated in Fig. 3. Even though the reference voltage is applied externally in the proposed design, its integrated implementation should not suppose

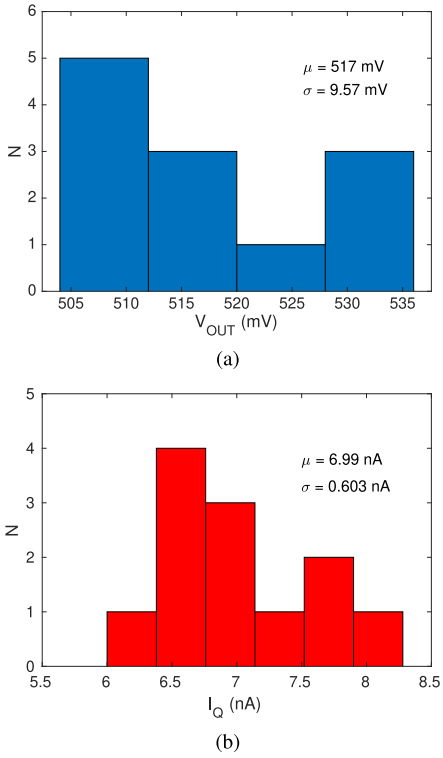

Fig. 5. Measured histograms of the LDO: (a) output voltage and (b) quiescent current.

a significant increase of the overall quiescent consumption, as a large variety of picoampere voltage references has been proposed in the literature [51]–[53]. Nevertheless, the loading effect of the proposed LDO on the voltage reference must be carefully considered, especially if the power consumption of the latter is intended to be kept to a minimum. When the input voltage of the LDO is reduced to 0.4 V and the reference voltage is set equal to 0.3 V the distribution of the output voltage of the regulator is 313.5±9.1 mV with a quiescent current of 6.69±0.513 nA.

The experimental DC characterization of the LDO is illustrated in Fig. 6. In particular, Fig. 6a shows the input/output transfer characteristic for different values of V_{REF}. It may be observed that the LDO starts operating from an input voltage as low as approximately 0.4 V. Beyond this level the value of V_{OUT} remains unchanged and equal to V_{REF}. The measured LS has been determined to be equal to 3.18±1.44 mV/V. Furthermore, the dependence of the output voltage, V_{OUT} with the load current, I_L, is depicted in Fig. 6b. As observed, the maximum load current for the case $V_{IN} = 600$ mV and $V_{REF} = 500$ mV is approximately equal to 570 μA. Besides, the load current may be increased with respect to this value for higher levels of V_{IN}. The LR was found to be equal to 4.77±0.66 mV/mA. Additionally, the DC input current through the reference terminal of the EA was measured and is depicted in Fig. 6c. In the PMOS bulk-driven transistors of the EA the bulk terminal, *n*-type, and the source diffusion, *p*-type, form a *pn* junction. Thus, when the voltage V_{REF} is close to V_{IN} the *pn* junction is reverse-biased and the corresponding current will be extremely small and positive (sourced to the terminal). Conversely, when V_{REF} is close to

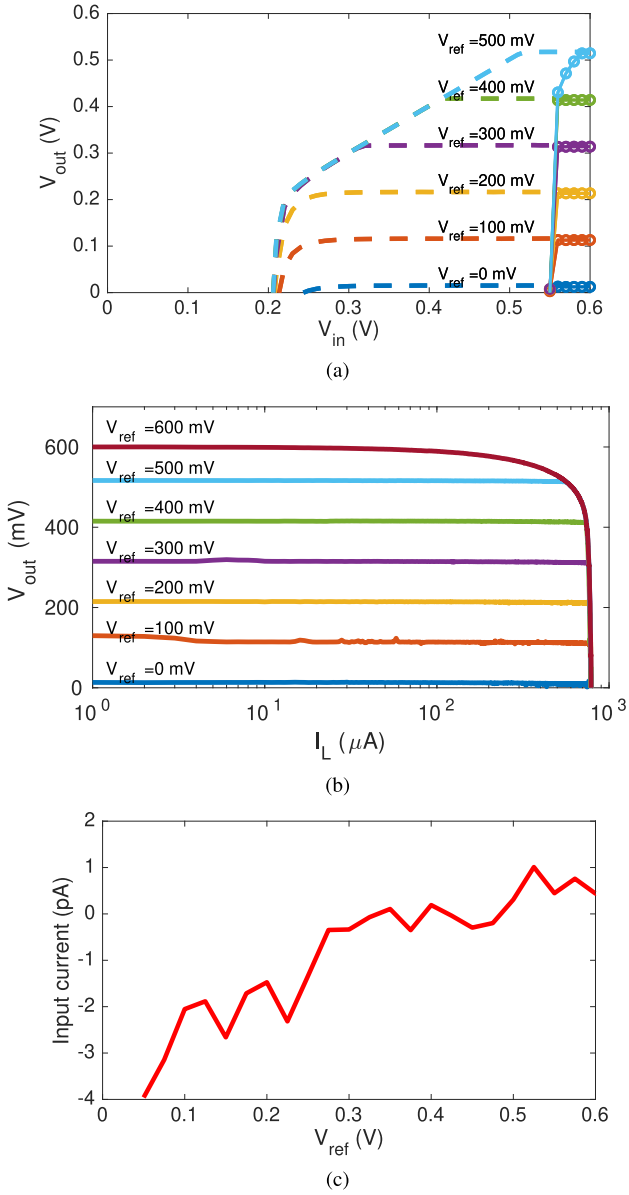

Fig. 6. Experimental DC characterization of the LDO: (a) V_{OUT} vs V_{IN} for $I_L = 100$ nA (dashed line) and $I_L = 500$ μA (circular dots line), (b) V_{OUT} vs I_L with $V_{IN} = 600$ mV and (c) input current through the reference terminal.

ground, the intrinsic diode is forward-biased and the current will become negative (sinked from the terminal) and will follow an exponential behavior. The extremely low current levels measured show that, despite using BD MOS transistors, the loading effect on the preceding stage, i.e., the voltage reference section generating V_{REF}, is negligible in most cases. In any case, the lower bound of the power consumption of the voltage reference will be limited by the loading imposed by the proposed BD CL-LDO. It is worth to mention that due to the small level of the input current, every DC measurement in Fig. 6c was obtained from the average of 10.000 different points.

The dynamic response of the proposed LDO has also been experimentally characterized. The inherently low value of the biasing currents used in the different stages of the voltage regulator lead to a very reduced bandwidth for the PSR, around

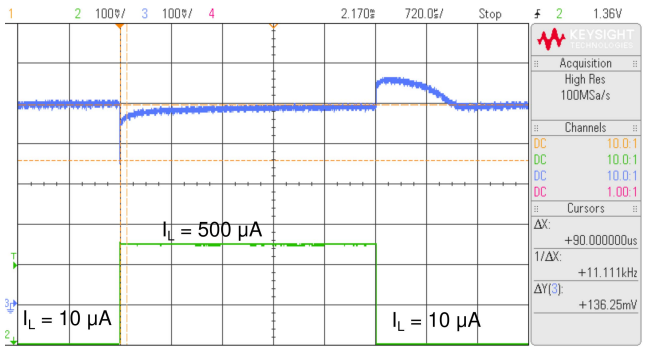

Fig. 7. Transient response of the LDO with $V_{IN} = 0.6$ V and $V_{REF} = 0.5$ V for I_L switched between 10 μA and 500 μA.

0.4 Hz in our case. Thus, the DC level of this metric had to be estimated from the value of the LS, due to evident limitations of the instrumentation used, leading to a value of approximately -50 dB. For frequencies higher than the bandwidth of the LDO, the PSR progressively increases until the maximum value is reached [27]. As it may be inferred from (13), the use of bulk-driven transistors in the EA leads to an increase of the PSR, fact that in our design has been counteracted by the selection of an unity gain feedback loop in the LDO, i.e., $\beta = 1$, as it has been already indicated. On the other hand, the transient response of the output voltage of the LDO, V_{OUT}, under a large variation of the load current, is illustrated in Fig. 7. The load current has been switched between values of 10 μA and 500 μA, although the time response of the voltage regulator has been proven to be stable for steps in the load current ranging from zero to 750 μA. As it may be observed, the low-to-high load current transition, determined by the high drive capability of the pass transistor, is very fast. Conversely, during the high-to-low transition of I_L the pass transistor is switched off and the bias transistor M_{Bout} has to discharge the output node, thus restoring the required level of V_{OUT}. The low-to-high and high-to-low response times have been experimentally determined to be equal to 92 μs and 915 μs, respectively.

A summary of the experimental response of the proposed LDO, illustrated in Fig. 3, is provided in Table II. The LDO has been characterized for $V_{IN} = 0.6$ V and $V_{REF} = 0.5$ V. Besides, in Table II the proposed LDO is also compared to other similar contributions found in the literature. In order to carry out an objective comparison, three different figures of merit (FoMs) have been used. The first of them is the widely used FoM_t, defined as (17), which contains the relationship between the transient response of the LDO, T_R, and the ratio of the quiescent current consumption over the load current range provided by the regulator, $I_Q/\Delta I_L$.

$$FoM_t = T_R \frac{I_Q}{\Delta I_L} \tag{17}$$

In order to consider the constraints imposed by a reduced supply voltage, a modification of the FoM_t was performed to obtain the FoM_{tV}, very similar to the one proposed in [37] and defined as

$$FoM_{tV} = T_R \frac{I_Q}{\Delta I_L} \cdot \left(\frac{V_{IN}}{V_{IN,max}} \right)^2 \tag{18}$$

TABLE II

SUMMARY OF THE EXPERIMENTAL RESULTS AND COMPARISON WITH THE STATE-OF-THE-ART

	This work	[30] TCASI'18	[32] TCASII'18	[34] TCASII'19	[35] ACCESS'19	[37] JSSC'20	[38] TCASI'20	[44] TCASII'20	[45] ISCAS'21
Technology	180 nm	65 nm	180 nm	180 nm	65 nm	55 nm	28 nm	28 nm	180 nm
Capacitor-less	yes	yes	yes	yes	yes	no	no	no (on-chip)	yes
Size (μm^2)	4310	4200	210000	31000	7000	42000	5500	8600	128000
V_{IN} (V)	0.6	1	1.6-1.8	1.2-1.8	1.2-2.5	0.8	0.4	0.9	3.4-5.6
V_{OUT} (V)	0.5	0.8	1.4-1.6	0.8-1.6	1-1.3	0.6	0.35	0.85	1.8
I_Q (nA)	6.99	30	133000	10800	9600	16	430	33000	11
I_L max (mA)	0.75	10	50	100	70	10	17	20	50
LS (mV/V)	3.18	-	2.67	10	3.84	0.5	2.32	17.5	0.86
LR (mV/mA)	4.77	1.22	0.194	0.081	0.29	1.05	0.51	0.26	0.2
PSR@10 Hz (dB)	-22.5@0 A -17@500 μA	-	-	-	-67‡@$_{\text{heavy load}}$	-75@1 nA -43@10 mA	-	-30@20 mA	-
PSR@10 kHz (dB)	-24@0 A 0@500 μA	-40@10.3 mA	-70@50 mA	-	-26‡@$_{\text{heavy load}}$	-100@1 nA -43@10 mA	-	-30@20 mA	-
FoM_t (ps)	1286	0.75†	51	22	247†	11.4	12531†	0.52	582
FoM_{tV} (ps)	40	0.042†	14.2	2.82	31	0.84	173†	0.031	582
Edge time ratio k^*	300	2000	3.5	1000	-	200	30†	1	-
FoM_v (μV)	570	2925	1545	20606	-	22.4	102	290400	-

† Estimated from the transient response ‡ Simulation result $k^* = \frac{I_L \text{ edge time}}{\text{Shortest edge of the comparative}}$

where $V_{IN,max}$ is the highest value of the minimum input voltages among the solutions to be compared. Indeed, when a low supply voltage is used, the size of the pass transistor must be increased to provide a given load current. This fact leads to an increase of the parasitic capacitance to be driven by the EA and, hence, to an increase of the response time [37], which is counteracted by the most right term in (18).

Another parameter widely used for comparison is the FoM_V in (19), which takes into account the voltage drop, ΔV_{out}, when a sudden change in the load current, ΔI_L, occurs, weighted by the quiescent current, I_Q, and by a term k which is the ratio between the current step edge time over the fastest current edge of the comparative [30].

$$FoM_V = k\Delta V_{out}\frac{I_Q}{\Delta I_L} \tag{19}$$

As can be seen in Table II, the regulator proposed in this work offers the smallest quiescent current occupying a relatively small silicon area, and is able to work with the lowest supply voltage of the comparative. On the negative side, the FoM_{tV} of the proposed approach is one of the highest because of the very low biasing currents used. Nevertheless, we achieve one of the best FoM_V because the LDO is able to maintain a moderate voltage drop against a variation in the load current, while the quiescent current is as small as 7 nA. The lowest FoM_{tV} is reported in [44], but I_Q becomes several orders of magnitude larger than in our proposal and a more advanced CMOS technology, of 28 nm, was used. On the other hand, the FoM_V in [44] is the highest of the comparative because the transient voltage drop has a value of 176 mV with a quiescent current consumption of 33 μA. The lowest FoM_V can be found in [37], where the reported quiescent current consumption is only 16 nA maintaining the transient voltage drop at load current steps in 70 mV, but the biasing current depends on the load current making the power consumption large at heavy load situations. Furthermore, the circuit requires an off-chip capacitor for stability, making the implementation not suitable for fully integrated systems.

V. CONCLUSION

An LDO with reduced input voltage requirements may be implemented by including BD MOS transistors in the input stage of the error amplifier. The capability of a BD transistor to decouple the biasing voltage and the signal voltage components allows properly setting the quiescent operating point and establishing an unitary feedback loop around the LDO simultaneously. As a result, the reference voltage, V_{REF}, and, consequently, the output voltage, V_{OUT}, may be swept over the entire voltage range from the negative rail to nearly the positive supply without the need of using a resistive feedback network. Besides, the minimum input voltage required for proper operation may be highly reduced. The design and fabrication of the proposed CL-LDO in standard 180-nm CMOS technology has allowed demonstrating that the voltage regulator is able to operate with input voltages as low as 0.4 V, while when $V_{IN} = 0.6$ V and $V_{REF} = 0.5$ V a maximum current of 0.75 mA may be delivered to the load with a total quiescent current of only 7.0 nA.

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