3D Simulations of Random Dopant and Metal Gate Workfunction Variability in an $In_{0.53}Ga_{0.47}As$ GAA MOSFET

N. Seoane, G. Indalecio, E. Comesaña, A. J. García-Loureiro, M. Aldegunde and K. Kalna

***Abstract*—We investigate the impact of random dopant and gate workfunction variability on sub-threshold characteristics of a 50 nm gate length, inversion-mode gate-all-around (GAA) $In_{0.53}Ga_{0.47}As$ MOSFET using a 3D finite-element (FE), quantum-corrected drift-diffusion (DD) device simulator calibrated to experimental data. We have studied threshold voltage, off-current, and sub-threshold slope variations. The workfunction variations on the sub-threshold characteristics dominate and decrease with the reduction in grain diameter. The simulated grain diameters of 10, 7 and 5 nm exhibit threshold voltage standard deviations of 52, 41 and 27 mV, respectively. These values are larger than those observed in TiN metal-gate Si FinFETs for a similar gate length. The impact of random dopant fluctuations is negligible when compared with bulk Si MOSFETs giving a threshold voltage spread of only 6 mV.**

***Index Terms*—Intrinsic parameter fluctuations, drift-diffusion, density gradient, III-V materials, gate-all-around MOSFETs.**

I. Introduction

As planar bulk Si MOSFETs reach their scaling limits, high mobility channel n-type MOSFETs based on III-V semiconductors have become intensively investigated [1], [2] as an option for the sub-16 nm Si CMOS technology [3]. The introduction of III-V semiconductors into the n-MOSFET channel calls for transistor architectures which benefit from their high mobility and injection velocity [4], neutralising the drawbacks [5] related to the lower density of states when compared to Si. In addition, a non-planar device architecture will likely be required to maintain electrostatic control. The demonstration of the first inversion-mode $In_{0.53}Ga_{0.47}As$ GAA FinFET by a top-down approach with atomic-layer deposited Al_2O_3/WN gate stacks [6] signals realisation of III-V channel FinFETs. Even though the GAA assures an excellent control of carriers in the channel, variability effects in the sub-threshold might limit their scaling and integration into the CMOS technology [7]. Furthermore, sub-threshold characteristics of III-V MOSFETs have always been a matter of great concern because of the small density of states leading to a large quantum capacitance and a potential increase in the leakage current [5]. In this letter, we study the sub-threshold variability in a III-V GAA FinFET addressing the impact of two major sources of intrinsic parameter fluctuations: the random dopant fluctuation (RDF) and the metal grains induced gate workfunction variability (WFV). We simulate fluctuations in the device threshold voltage, the off-current, and the sub-threshold slope using 3D FE DD device simulations [8], that incorporate the quantum confinement effects via an optimised FE density gradient (DG) approach for multi-gate transistors [9].

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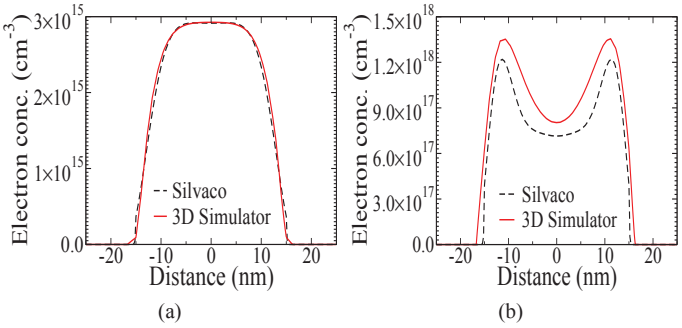


Fig. 1. Electron concentration in the middle of the channel at V_G=-0.9 (a) and -0.5 V (b) obtained from 3D DD-DG simulations and the 2D SP solver.

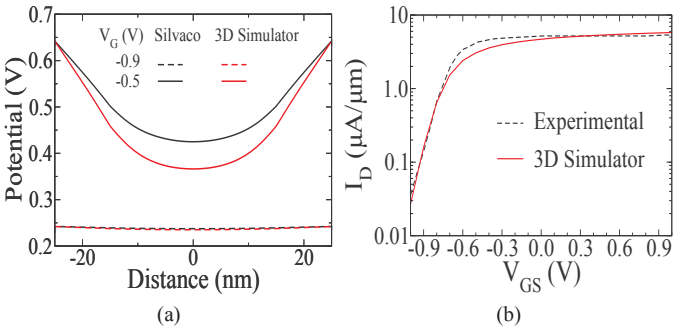
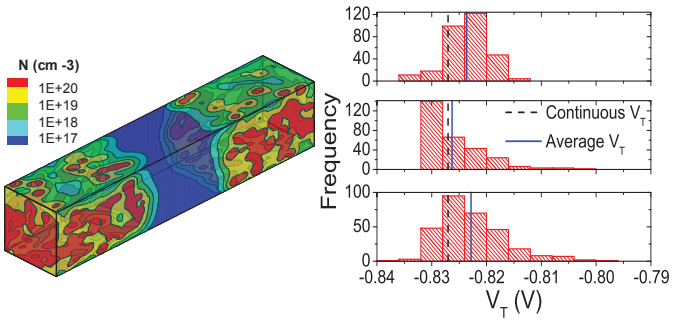


Fig. 2. (a) Potential in the middle of the channel from 3D DD-DG simulations and SP solver at gate biases of -0.9 and -0.5 V. (b) I_D-V_G characteristics from the 3D DD-DG simulator against experimental data at V_D=0.05 V.

II. Device structure and calibration process

The device has a 50 nm gate length $In_{0.53}Ga_{0.47}As$ channel, p-doped to 2x10^{16}cm^{-3}, with a 30 × 30 nm^2 cross-section, a 10 nm thick Al_2O_3 encapsulation layer and 50 nm wide n-doped source/drain (S/D) regions. The doping profile was generated via the atomistic Monte Carlo simulation of ion implantation in Sentaurus Process [10]. The modelling of the S/D Si implantation was performed at an energy of 20 keV and a dose of 10^{14} cm^{-2}; the dopant activation at 600 °C for 15 s in nitrogen ambient. Quantum corrections are calibrated via the DG parameters used in our 3D DD-DG simulator against Silvaco Atlas 2D Schrödinger-Poisson (SP) solver across the



(a) (b)

Fig. 3. (a) Electron concentration in the $In_{0.53}Ga_{0.47}As$ region for a pattern of RDs at V_G=V_T and V_D=0.05 V. (b) Distribution of threshold voltages due to the RDF in the n-type doped S/D regions (top), the p-type doped channel (middle), and in the both S/D and channel of the device (bottom).

middle of the channel for a range of gate biases. Figs. 1(a) and 1(b) show a comparison of 1D electron concentrations along the y-axis at V_G=-0.9 and -0.5 V, respectively. The corresponding electrostatic potential is shown in Fig. 2(a). The DG approach accurately reproduces the shape of the electron density in the channel, especially at large negative gate biases. The electron effective masses in the $In_{0.53}Ga_{0.47}As$ region and in the oxide are used as calibration parameters. At a very low gate bias (such as -0.9 V), the electron effective masses were determined to be $0.014m_0$ in x-direction and $0.041m_0$ in y and z-directions and the effective mass for the oxide was set to $0.1m_0$. However, for larger biases (-0.5 V and above), the electron effective masses were determined to be $0.014m_0$ in x, y and z-directions and the effective mass for the oxide was set to $0.2m_0$ showing that the calibration is not possible with a single set [11]. After the DG parameters have been adjusted, the I_D-V_G characteristics obtained from the 3D simulations have been calibrated against experimental data [6] at a drain bias of 0.05 V, as seen in Fig. 2(b) on a logarithmic scale, providing a very good resolution of the sub-threshold region. In the calibration process, we have used a low field mobility model specific for III-V compounds [12] and the transferred electron mobility model for high electric fields [13].

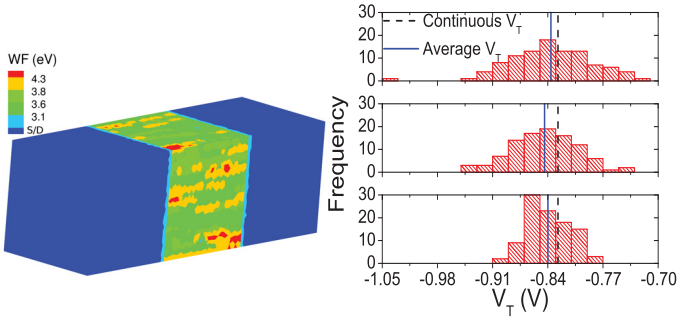
III. Random Dopant Induced Variability

To investigate the variability introduced by the presence of random discrete dopants (RDs) in the n-type doped S/D regions and p-type doped channel, we simulate an ensemble of 300 different $In_{0.53}Ga_{0.47}As$ GAA MOSFETs. We obtain the devices using a rejection technique from the device with the doping profile generated by Sentaurus Process. The dopants are placed on an atomistic grid defined by the positions of the atoms. The charge associated with this distribution is mapped to the tetrahedral mesh using a cloud-in-cell algorithm creating an 'atomistic' electron density profile, see Fig. 3(a). Initially, we have analysed the influence of the n-type and p-type doping on the RDs induced threshold voltage fluctuations. Fig. 3(b) shows the threshold voltage variability due to the n-type dopants in the S/D regions (top figure), the p-type dopants distributed along the channel (middle figure), and the combined effect of both the n-type and p-type dopants (bottom figure). The mean of the threshold voltage distributions and

TABLE I

The mean values and standard deviations of threshold voltage (V_T), off-current (I_{off}) and sub-threshold slope (SS) due to n-type and p-type RDF and WFV for 10, 7 and 5 nm metal grain sizes obtained from the statistical analysis.

Source / Source	$\langle V_T \rangle$ (mV)	σV_T (mV)	$\langle \log_{10}(I_{off}) \rangle$ (μA/μm)	$\sigma \log_{10}(I_{off})$ (μA/μm)	$\langle SS \rangle$ (mV/dec)	σSS (mV/dec)
RDF	-823	5.90	-5.68	0.0937	128	2.11
10	-836	52.0	-5.54	0.395	136	38.3
WFV 7	-844	41.4	-5.48	0.308	135	23.1
(nm) 5	-840	26.6	-5.51	0.203	133	17.0



(a) (b)

Fig. 4. (a) Example of the metal gate WFV for a 5 nm grain size. (b) Distribution of threshold voltages due to metal gate WFV for three different grain sizes: 10 nm (top), 7 nm (middle), and 5 nm (bottom).

the corresponding continuous doping value (V_{T0}=-0.827 V) are also shown for comparison. When we consider just p-type induced fluctuations, there might occur an extreme case when there are no dopants inside the channel. In this case, the current will be at its maximum and the V_T will reach the lowest limit (see Fig. 3(b) middle). Even though the average number of p-type dopants (3) is much smaller than the n-type ones (2116), the p-type dopants are located in the channel, and thus they have a larger impact on the current flow. Therefore, the spread in the threshold voltages (σV_T) due to p-type RDs, 5.5 mV, is much larger than due to the n-type ones, 3.6 mV [14]. Table I collects the average values and standard deviations obtained from the variability study of threshold voltage, off-current, and sub-threshold slope due to the presence of RDs in the both n-type doped S/D regions and p-type doped channel. The RD induced threshold voltage shift, $\langle V_T \rangle$-V_{T0}, is 4.2 mV, and a standard deviation in the threshold voltage is 5.9 mV. These values are noticeably lower than those observed in the equivalent, 50 nm gate length bulk Si MOSFETs [15] (with σV_T and $\langle V_T \rangle$-V_{T0} over 70 mV). In the presence of RDs, there is less than 1% shift in the sub-threshold slope and off-current when compared to the continuous doping values (SS_0=129 mV/dec and $\log_{10}(I_{off0})$=-5.61 μA/μm). Furthermore, the standard deviations of the SS and I_{off} are very small, of around 2 mV/dec and 0.1 μA/μm, respectively.

IV. Metal Gate Workfunction Variability

To model the dependence of the gate workfunction (GWF) on the granularity, we define four possible orientations of the grains with GWF of 3.6, 3.8, 4.3 and 3.1 eV, and probabilities of occurrence 65%, 15%, 15% and 5%, respectively [16]. We select the GWF values by scaling the experimental ones to adjust them to the GWF set-up (3.71 eV) during the calibration

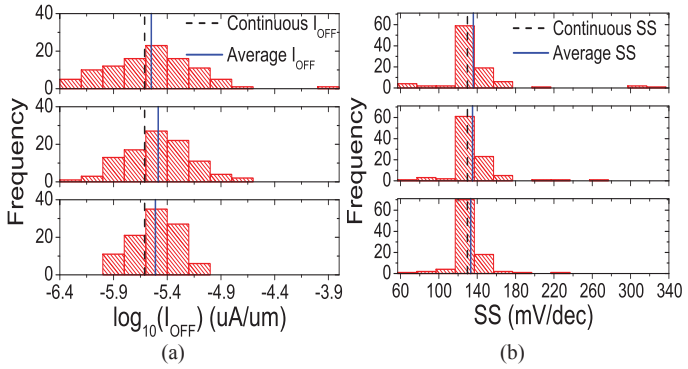


Fig. 5. (a) Distribution of off-currents and (b) sub-threshold slopes due to gate WFV for 10 nm (top), 7 nm (middle), and 5 nm (bottom) grain sizes.

of the I_D-V_G characteristics. We then calculate a Voronoi diagram of a set of randomly generated points, which varies the size and shape of the grains as in realistic crystalline structures. We assign a certain orientation to each polygon based on the experimental probability of occurrence [17]. We consider three different average grain sizes (10, 7 and 5 nm), and generate 100 different workfunction patterns for each grain size. An example of a GWF generated for a 5 nm grain size is shown in Fig. 4(a). Figs 4 (b), 5(a) and 5(b) show the distribution of threshold voltages, off-currents and sub-threshold slopes due to WFV for grain sizes of 10 nm (top figures), 7 nm (middle figures) and 5 nm (bottom figures), respectively. The mean of the distribution and the value for uniform GWF for each case are also shown for comparison. The statistical WFV for the three grain sizes is summarised in Table I. The standard deviation of three figures of merit decreases with reducing grain size. For example, the grain size reduction from 10 nm to 7 nm and 5 nm reduces the spread in the both V_T and I_{off} approximately 20% and 49%, respectively. Decrease in the standard deviation is more pronounced for the sub-threshold slope, with 40% decrease for the 7 nm and 55% for the 5 nm grain size. The threshold voltage and off-current shift less than 3% when compared to the uniform GWF model and the sub-threshold slope around 5%. σV_T for the 10 nm grain size (over 50 mV) is much larger than the one observed in the equivalent gate length TiN metal-gate Si FinFET for a 20 nm grain size (around 30 mV) [18]. For this TiN metal-gate Si FinFET, the difference in workfunctions between the two possible grain orientations is around 200 mV [16]. The $In_{0.53}Ga_{0.47}As$ GAA FinFET with a WN metal gate has the largest difference in workfunctions between the metal grain orientation with the highest probability of occurrence (65%) and other possible grain orientations around 700 mV. Consequently, the WFV in the $In_{0.53}Ga_{0.47}As$ FinFET is larger due to this larger spread in workfunctions of different grain orientations than those present in the Si FinFET.

V. Conclusion

We have studied the V_T, I_{off} and SS variability induced by RD and GWF for an inversion-mode $In_{0.53}Ga_{0.47}As$ GAA FinFET. The WFV has a considerable impact on the sub-threshold characteristics of the device, which strongly depends on the grain size. For the 10 nm grain size σV_T is over 50 mV, a much larger value than in the equivalent gate length Si FinFET with a 20 nm metal grain size (σV_T around 30 mV) [18]. RDF are secondary because σV_T, $\sigma \log_{10}(I_{off})$, and σSS due to the metal gate WFV are at least 4, 6 and 8 times larger than the respective σ's due to RDs.

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