

# Impact of gate edge roughness variability on FinFET and gate-all-around nanowire FET

G. Espiñeira, D. Nagy, G. Indalecio, A. J. García-Loureiro, K. Kalna and N. Seoane

**Abstract**—The effect of gate edge roughness (GER) in the sub-threshold region is studied for two state-of-the-art architectures: a 10.7 nm Si FinFET and a 10 nm Si gate-all-around (GAA) nanowire (NW) FET using an in-house 3D quantum corrected drift-diffusion simulation tool. The GER is applied to the device gate using characteristic values of root mean square amplitude (RMS) and correlation length (CL). The GER induced variability results in a standard deviation ( $\sigma$ ) for the threshold voltage ( $V_T$ ) of 7 mV for the FinFET when CL/Gate Perimeter = 0.66 and RMS = 0.80 nm, which is 20% greater than that of the GAA NW FET. GER is a less damaging source of variability than metal grain granularity (MGG), line edge roughness (LER) and random dopants (RD) for both devices. When compared to LER variations,  $\sigma V_T$  due to the GER is 62% and 86% lower for the FinFET and GAA NW FET, respectively. However, although GER affects more the FinFET than the GAA NW FET, the combined variability effect of GER, MGG, LER and RD ( $\sigma V_{T,comb}$ ) on the FinFET is 30 mV, a value approximately 50% smaller than that of the GAA NW FET.

**Index Terms**—FinFET, Gate-all-around nanowire FET, Gate Edge Roughness, Variability

## I. INTRODUCTION

FinFETs are the preferred device architecture in industry for the 10 nm technology node as they fulfill the requirements for both gate control and suppression of short-channel effects [1][2]. For future technology nodes, other multi-gate architectures need to be considered to be able to keep up with industry requirements [3][4]. In this context, the GAA NW FET presents itself as a viable substitute to previous architectures as its cylindrical geometry further improves the gate control [5]. However, due to the progressive scaling of CMOS technology, variability issues intensify, making a necessity to develop means to minimize them [6]. During the transistor fabrication, as a result of lithography and etching processes, gate edge roughness (GER) might be a considerable source of variability affecting device performance as it does not scale down with technology [7]. Previous works covering the effect of GER for bulk MOSFETs [8] and FinFETs [9] have been presented but they lack a study comparing the effect of this variability in state-of-the-art FinFET and GAA NW FETs. In this work, we present a comparative study of the impact of GER variability on a 10.7 nm gate length Si FinFET and a 10 nm gate length Si GAA NW FET. Two of the main figures of merit (FoM) describing the sub-threshold region, the threshold

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Table I  
DEVICE DIMENSIONS AND MAIN FOM FOR THE 10.7 NM GATE LENGTH FINFET AND THE 10 NM GATE LENGTH GAA NW FET.

| Symbol  | FinFET    | GAA NW FET |
|---|-----------|------------|
|   | 10.7 nm   | 10 nm      |
| Gate length ( $L_G$ )[nm]                       | 10.7      | 10.0       |
| S/D length ( $L_{S/D}$ )[nm]                    | 10.7      | 14.0       |
| Channel width ( $W_{CH}$ )[nm]                  | 5.8       | 5.7        |
| Channel height ( $H_{CH}$ )[nm]                 | 15.0      | 7.17       |
| Equivalent oxide thickness (EOT)[nm]            | 0.62      | 0.80       |
| Channel p-type doping ( $N_{CH}$ )[ $cm^{-3}$ ] | $10^{15}$ | $10^{15}$  |
| S/D n-type doping ( $N_{S/D}$ )[ $cm^{-3}$ ]    | $10^{20}$ | $10^{20}$  |
| S/D doping lateral straggle ( $\sigma_x$ )      | 3.45      | 3.23       |
| S/D doping lateral peak ( $x_p$ )[nm]           | 11.0      | 7.8        |
| Channel perimeter [nm]                          | 35.8      | 20.3       |
| Gate perimeter [nm]                             | 45.4      | 25.0       |
| SS [mV/dec]                                     | 77        | 71         |
| $V_T$ [V]                                       | 0.255     | 0.250      |
| $I_{OFF}$ [ $\mu A/\mu m$ ]                     | 0.0341    | 0.0267     |
| $I_{ON}$ [ $\mu A/\mu m$ ]                      | 1774      | 1770       |
| $I_{ON}/I_{OFF}$ ( $\times 10^4$ )              | 5.202     | 6.629      |

voltage ( $V_T$ ) and the OFF current ( $I_{OFF}$ ), have been studied using an in-house-built 3D density gradient quantum corrected drift-diffusion (DG-DD) simulator [10]. The obtained GER results are compared to the some of the major variability sources affecting these devices: MGG [11][12], LER [13][14] and RD [15][16]. This information could help in the design of fluctuation resistant architectures.

## II. DEVICE STRUCTURE AND SIMULATION METHODOLOGY

The devices that have been used for this study are two state-of-the-art transistors based on experimental data [17][18] scaled down following the ITRS guidelines [19]. The main dimensions and doping values can be seen in Table I. The device channel has been uniformly doped whereas the source/drain (S/D) regions have a Gaussian doping. These Gaussian doping profiles, reverse engineered from experimental data [20] and scaled accordingly, are characterized by the S/D doping lateral straggle ( $\sigma_x$ ), that describes the slope of Gaussian profile, and the S/D doping lateral peak ( $x_p$ ), that indicates the position where the Gaussian decay starts measured from the middle of the channel (see Table I). Our in-house-built 3D DG-DD simulator is based on the finite element (FE) approach that accurately describes complex three-dimensional geometries [10]. The DG-DD includes the Caughney and Thomas doping dependent low-field electron mobility model [21], combined with lateral (saturation velocity) and perpendicular (critical field) electric field models [22]. The DG quantum

Table II

CALIBRATION PARAMETERS:  $v_{\text{sat}}$  IS THE SATURATION VELOCITY,  $E_{\text{CN}}$  IS THE PERPENDICULAR CRITICAL ELECTRIC FIELD,  $m_x$  AND  $m_{y,z}$  ARE THE DG ELECTRON MASSES IN THE TRANSPORT AND CONFINEMENT DIRECTIONS.

|                         | FinFET 10.7 nm     | GAA NW 10 nm       |
|-------------------------|--------------------|--------------------|
| $v_{\text{sat}}$ [cm/s] | $1.00 \times 10^9$ | $1.30 \times 10^7$ |
| $E_{\text{CN}}$ [V/cm]  | $5.00 \times 10^4$ | $9.95 \times 10^5$ |
| $m_x$ [ $m_0$ ]         | 0.25               | 0.50               |
| $m_{y,z}$ [ $m_0$ ]     | 0.10               | 0.10               |

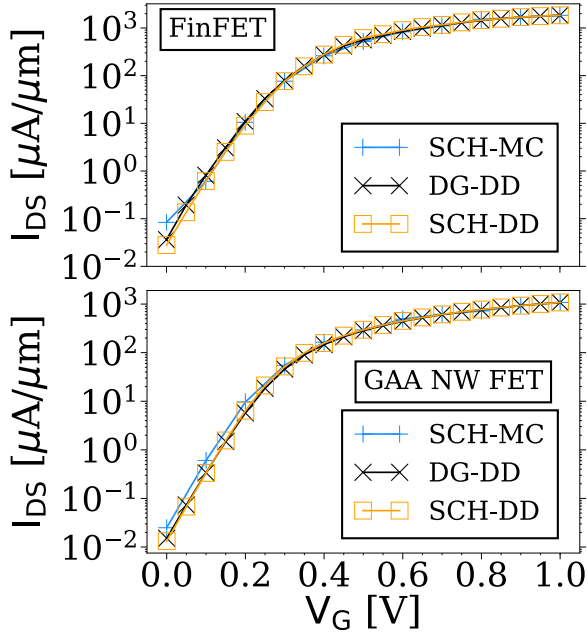


Figure 1. DG-DD simulated  $I_D$ - $V_G$  characteristics for: the FinFET (top) and the GAA NW FET (bottom), compared against SCH-DD and to SCH-MC simulations, at  $V_{D,\text{sat}} = 0.70$  V.

corrections use calibrated electron effective masses to account for source-to-drain tunneling and quantum confinement [23]. All the calibration parameters are summarised in Table II.

The DG-DD  $I_D$ - $V_G$  characteristics have been meticulously calibrated (see Fig. 1) at a high drain bias ( $V_{D,\text{sat}}$ ) of 0.7 V. They have been matched to DD simulations including anisotropic Schrödinger equation (SCH) based quantum corrections (SCH-DD) in the sub-threshold region and to SCH quantum-corrected Monte Carlo simulations (SCH-MC) [24] in the on region, as the SCH-MC may produce noisy results at very low gate voltages. In order to compare both architectures from the performance point of view, Table I presents the main FoM that characterize these benchmark devices. A constant current criteria of  $I_{\text{DCC}} = 32.6$  [ $\mu\text{A}/\mu\text{m}$ ] has been used to obtain  $V_T$  for both devices.  $I_{\text{ON}}$  has been extracted as the drain current at  $V_G = V_T + V_{D,\text{sat}}$  V. The sub-threshold slope (SS) is slightly lower ( $\approx 8\%$ ) for the GAA NW FET which translates to a faster switching speed than that of the FinFET. The GAA NW FET shows lower  $I_{\text{OFF}}$  (by 22%) and similar  $I_{\text{ON}}$  (<1% lower) compared to the values yielded by the FinFET, resolving in less power leakage. As a conclusion, the GAA NW FET outperforms the FinFET by

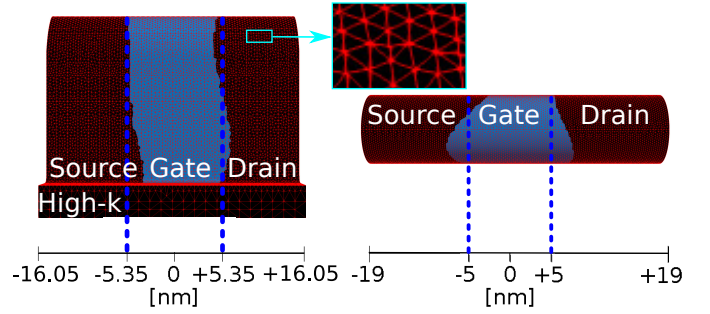


Figure 2. FinFET [17] and GAA NW FET [18] showing a GER deformed gate. A close-up view of the FE mesh used is also shown.

a 20% larger  $I_{\text{ON}}/I_{\text{OFF}}$  ratio. After the ideal, non-deformed device has been calibrated to produce sound results, the GER is applied to the gate of the device. GER has been designed similarly to the line edge roughness (LER) using the Fourier synthesis methodology as previously explained in [7][25]. To parametrize the GER, two variables have been defined: the correlation length (CL), that models the width of the Gaussian filter on the gate long edges, and the root mean square (RMS) height that quantifies the variations in the width of the gate in the transport direction. To properly capture the effect of GER, different CL and RMS values were simulated which were observed experimentally and also shown to produce the greatest variability results [18][26][27]. For each set of CL and RMS parameters, an ensemble of 300 simulations has been performed to obtain a statistically significant prediction on the behaviour of the device. Fig. 2 shows an example of the two studied devices with their gates affected by GER.

### III. GER VARIABILITY

In this section, we first study the effect of GER in the sub-threshold region for the 10.7 nm gate length Si FinFET and the 10 nm gate length Si GAA NW FET and later we present a comparison between these results and other variability sources. Fig. 3 (top) shows  $\sigma V_T$  and  $\sigma \log_{10}(I_{\text{OFF}})$  versus the CL for a fixed RMS of 0.80 nm. The CL has been normalized by the gate perimeter (see values in Table I), in order to perform a fair comparison of the results. Note that, for both devices, the variability increases linearly with the CL/Gate Perimeter. Results show that, in the sub-threshold region, the GAA NW FET is more resilient to GER than the FinFET. For instance, when  $\text{CL}/\text{Gate Perimeter} = 0.66$ ,  $\sigma V_T$  and  $\sigma \log_{10}(I_{\text{OFF}})$  are, respectively, 20% and 11% larger for the FinFET than for the GAA NW FET. A comparison of the GER variability versus the RMS with a constant CL/Gate Perimeter of 0.44 for our benchmark devices can be seen in Fig. 3 (bottom). As previously reported for LER [26], GER variability will increase with the RMS. We obtain maximum variability values at a RMS value of 1.0 nm, where  $\sigma V_T$  and  $\sigma \log_{10}(I_{\text{OFF}})$  are 34% and 18% larger for the FinFET than for the GAA NW FET, respectively. A reason for the smaller variability yielded by the GAA NW FET is that the GER profiles have to be periodic as the device has a continuous gate whereas, for the FinFET, the trigate structure does not require this boundary condition. Similarly, a decrease in the MGG variability of

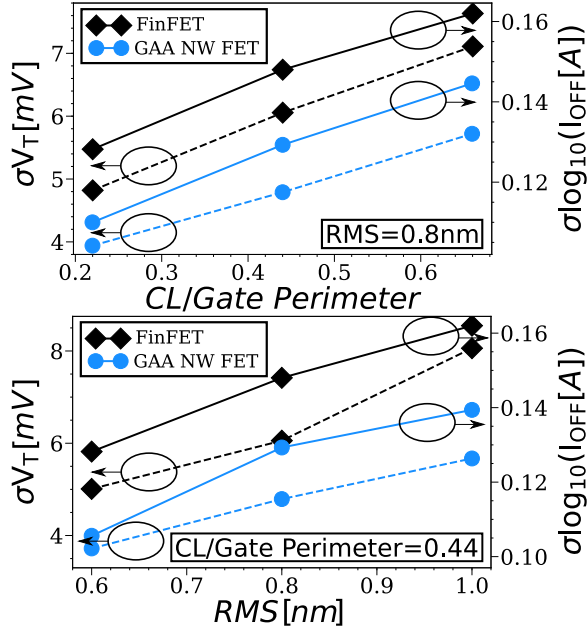


Figure 3. GER variability as a function of: the CL/Gate Perimeter (top) and RMS (bottom) for  $\sigma V_T$  (left) and  $\sigma \log_{10}(I_{OFF})$  (right) at  $V_{D,sat} = 0.70$  V.

GAA NW FETs was previously reported when using periodic Voronoi patches [28].

Finally, we have compared the impact of GER (CL/Gate Perimeter = 0.66, RMS = 0.80 nm) against three of the major variability sources affecting multi-gate devices: MGG, LER and RD. The results for MGG (grain size = 5.0 nm) and LER (CL = 20 nm, RMS  $\approx$  0.80 nm) are taken from previously published DG-DD simulations [23][25], whereas the RD variability is explicitly simulated for this study following the methodology from [29]. Fig 4 shows the impact on  $\sigma V_T$  (top) and on  $\sigma \log_{10}(I_{OFF})$  (bottom) of the aforementioned four sources of variability and their combined effect for both the FinFET and GAA NW FET. Comparatively, the GER is the least damaging source of variability affecting  $\sigma V_T$  and  $\sigma \log_{10}(I_{OFF})$  for both devices.  $\sigma V_T$  produced by GER is 49% and a 72% smaller than the corresponding RD variations for the FinFET and the GAA NW FET, respectively. The RD variation is 30% larger for the GAA NW FET than for the FinFET, which partly due to the NW's longer S/D regions and to the different lateral peak positions of the Gaussian doping profiles (see  $L_{S/D}$  and  $x_p$  in Table I). If  $L_{S/D}$  for the GAA NW FET is similar to the FinFET's, there is a 13% decrease in the RD variation. Moreover,  $x_p$  is lower for the GAA NW FET, implying that the Gaussian doping will penetrate further into the channel leading to the aforementioned increase in variability. The GER variability for  $\sigma V_T$  is around 62% and 86% smaller for the FinFET and the GAA NW FET, respectively, than the LER variations, which is the most damaging source of variability. The LER variability is larger for the GAA NW FET than the FinFET because of its smaller channel height leading to a stronger confinement limiting the device conductivity in the transport direction [25]. Moreover, although the impact of GER on the FinFET is greater than

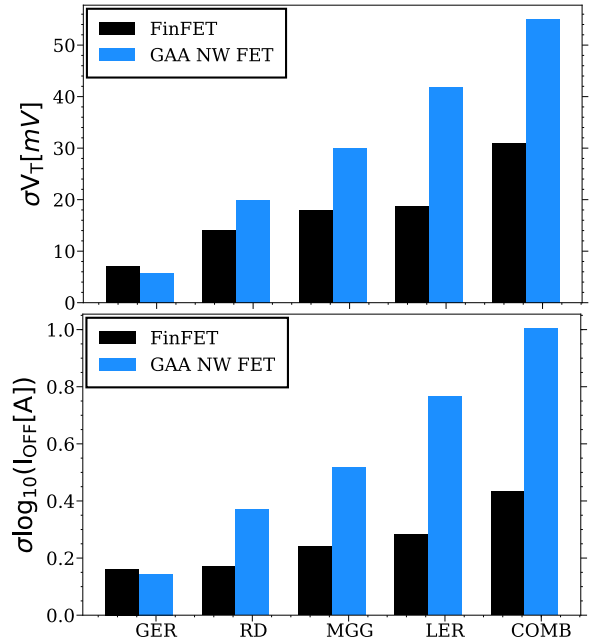


Figure 4. GER variability for  $\sigma V_T$  (top) and  $\sigma \log_{10}(I_{OFF})$  (bottom) compared to other major sources of variability (MGG [25], LER [23][25] and RD) and their combined effect (COMB) at  $V_{D,sat} = 0.70$  V.

on the GAA NW FET, the statistical combination of the four sources shows that the FinFET device is more resilient to the effect of variability (with a  $\sigma V_{T,comb} = 30$  mV and a  $\sigma \log_{10}(I_{OFF,comb}) = 0.44$ ), a value 46% lower for  $\sigma V_T$  and 56% lower for  $\sigma \log_{10}(I_{OFF})$  than that of the GAA NW FET.

#### IV. CONCLUSIONS

We have studied the impact of GER variability on the performance of a 10.7 nm gate length Si FinFET and a 10 nm gate length Si GAA NW FET using two of the main FoM ( $V_T$ ,  $I_{OFF}$ ) in the sub-threshold region. The GER induces standard deviations of  $\sigma V_T = 7$  mV and  $\sigma \log_{10}(I_{OFF}) = 0.16$  for the FinFET when CL/Gate Perimeter = 0.66 and RMS = 0.80 nm, which are around 20% and 11% greater than those of the GAA NW FET. Moreover, we compared the GER variability versus MGG, LER and RD, yielding up to 62% lower impact for the FinFET and 86% for the GAA NW FET for  $\sigma V_T$ . Finally, even though the GER impact is greater on the FinFET, this device is more resilient to the combined effect of variability with results approximately 50% lower ( $\sigma V_{T,comb} = 30$  mV and  $\sigma \log_{10}(I_{OFF,comb}) = 0.44$ ) compared to the ones obtained from the GAA NW FET.

## REFERENCES

- [1] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320–2325, Dec 2000. doi: 10.1109/16.887014
- [2] J. Colinge, "Multi-gate SOI MOSFETs," *Microelectronic Engineering*, no. 9, pp. 2071 – 2076, Sept. 2007. doi: <https://doi.org/10.1016/j.mee.2007.04.038>
- [3] Y. Liu, T. Matsukawa, K. Endo, M. Masahara, K. Ishii, S. i. O'uchi, H. Yamauchi, J. Tsukada, Y. Ishikawa, and E. Suzuki, "Advanced Fin-FET CMOS Technology: TiN-Gate, Fin-Height Control and Asymmetric Gate Insulator Thickness 4T-FinFETs," in *Proc. IEEE Electron Devices Meeting (IEDM)*, Dec. 2006. doi: 10.1109/IEDM.2006.346953 pp. 1–4.
- [4] U. K. Das, G. Eneman, R. S. R. Velampati, Y. S. Chauhan, K. B. Jinesh, and T. K. Bhattacharyya, "Consideration of UFET Architecture for the 5 nm Node and Beyond Logic Transistor," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1129–1135, Dec. 2018. doi: 10.1109/JEDS.2018.2868686
- [5] J.-S. Yoon, T. Rim, J. Kim, M. Meyyappan, C.-K. Baek, and Y.-H. Jeong, "Vertical gate-all-around junctionless nanowire transistors with asymmetric diameters and overlap lengths," *J. Appl. Phys.*, vol. 105, no. 10, p. 102105, Sept. 2014. doi: 10.1063/1.4895030
- [6] IRDS. (2017) International roadmap for devices and systems: Beyond CMOS. [Online]. Available: <https://irds.ieee.org/roadmap-2017>
- [7] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1254–1260, May 2003. doi: 10.1109/TED.2003.813457
- [8] S. Xiong and J. Bokor, "A simulation study of gate line edge roughness effects on doping profiles of short-channel MOSFET devices," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 228–232, Feb 2004. doi: 10.1109/TED.2003.821563
- [9] X. Wang, A. R. Brown, B. Cheng, and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs," in *Proc. IEEE Electron Devices Meeting (IEDM)*, Dec 2011. doi: 10.1109/IEDM.2011.6131494 pp. 5.4.1–5.4.4.
- [10] A. J. Garcia-Loureiro, N. Seoane, M. Aldegunde, R. Valin, A. Asenov, A. Martinez, and K. Kalna, "Implementation of the Density Gradient Quantum Corrections for 3-D Simulations of Multigate Nanoscaled Transistors," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 6, pp. 841–851, Jun 2011. doi: 10.1109/TCAD.2011.2107990
- [11] S. Chou, M. Fan, and P. Su, "Investigation and Comparison of Work Function Variation for FinFET and UTB SOI Devices Using a Voronoi Approach," *IEEE Trans. Electron Devices*, vol. 60, no. 4, pp. 1485–1489, April 2013. doi: 10.1109/TED.2013.2248087
- [12] H. Nam, C. Shin, and J. Park, "Impact of the Metal-Gate Material Properties in FinFET (Versus FD-SOI MOSFET) on High- $\kappa$ /Metal-Gate Work-Function Variation," *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 4780–4785, Nov 2018. doi: 10.1109/TED.2018.2872586
- [13] R. Wang, X. Jiang, T. Yu, J. Fan, J. Chen, D. Z. Pan, and R. Huang, "Investigations on Line-Edge Roughness (LER) and Line-Width Roughness (LWR) in Nanoscale CMOS Technology: Part II Experimental Results and Impacts on Device Variability," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3676–3682, Nov 2013. doi: 10.1109/TED.2013.2283517
- [14] X. Jiang, R. Wang, R. Huang, and J. Chen, "Simulation of correlated line-edge roughness in multi-gate devices," in *SISPAD*, Sept 2013. doi: 10.1109/SISPAD.2013.6650590 pp. 123–126.
- [15] C. Millar, D. Reid, G. Roy, S. Roy, and A. Asenov, "Accurate Statistical Description of Random Dopant-Induced Threshold Voltage Variability," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 946–948, Aug 2008. doi: 10.1109/LED.2008.2001030
- [16] A. S. Spinelli, C. M. Compagnoni, and A. L. Lacaíta, "Random Dopant Fluctuation and Random Telegraph Noise in Nanowire and Macaroni MOSFETs," in *Proc. European Solid-State Device Research Conference (ESSDERC)*, Sept 2018. doi: 10.1109/ESSDERC.2018.8486871 pp. 230–233.
- [17] V. S. Basker, T. Standaert, H. Kawasaki, C. C. Yeh, K. Maitra, T. Yamashita, J. Faltermeier, H. Adhikari, H. Jagannathan, J. Wang, H. Sunamura, S. Kanakasabapathy, S. Schmitz, J. Cummings, A. Inada, C. H. Lin, P. Kulkarni, Y. Zhu, J. Kuss, T. Yamamoto, A. Kumar, J. Wahl, A. Yagishita, L. F. Edge, R. H. Kim, E. McLellan, S. J. Holmes, R. C. Johnson, T. Levin, J. Demarest, M. Hane, M. Takayanagi, M. Colburn, V. K. Paruchuri, R. J. Miller, H. Bu, B. Doris, D. McHerron, E. Leobandung, and J. O'Neill, "A 0.063  $\mu\text{m}^2$  FinFET SRAM cell demonstration with conventional lithography using a novel integration scheme with aggressively scaled fin and gate pitch," in *Proc. VLSI Technol. (VLSIT) Symp.*, Jun. 2010. doi: 10.1109/VLSIT.2010.5556135 pp. 19–20.
- [18] S. Bangsaruntip, K. Balakrishnan, S. L. Cheng, J. Chang, M. Brink, I. Lauer, R. L. Bruce, S. U. Engelmann, A. Pyzyna, G. M. Cohen, L. M. Gignac, C. M. Breslin, J. S. Newbury, D. P. Klaus, A. Majumdar, J. W. Sleight, and M. A. Guillorn, "Density scaling with gate-all-around silicon nanowire MOSFETs for the 10 nm node and beyond," in *Proc. IEEE Electron Devices Meeting (IEDM)*, Dec. 2013. doi: 10.1109/IEDM.2013.6724667 pp. 526–529.
- [19] ITRS. (2016) International Technology Roadmap for Semiconductors. [Online]. Available: <http://www.itrs2.net/>
- [20] M. Aldegunde, A. J. Garca-Loureiro, and K. Kalna, "3D Finite Element Monte Carlo Simulations of Multigate Nanoscale Transistors," *IEEE Trans. on Electron Devices*, vol. 60, no. 5, pp. 1561–1567, May 2013. doi: 10.1109/TED.2013.2253465
- [21] D. M. Caughey and R. E. Thomas, "Carrier Mobilities in Silicon Empirically Related to Doping and Field," in *Proc. IEEE*, vol. 55, no. 12, Dec. 1967. doi: 10.1109/PROC.1967.6123 pp. 2192–2193.
- [22] K. Yamaguchi, "Field-dependent mobility model for two-dimensional numerical analysis of MOSFET's," *IEEE Trans. Electron Devices*, vol. 26, no. 7, pp. 1068–1074, Jul. 1979. doi: 10.1109/T-ED.1979.19547
- [23] M. A. Elmessary, D. Nagy, M. Aldegunde, N. Seoane, G. Indalecio, J. Lindberg, W. Dettmer, D. Perić, A. J. Garcia-Loureiro, and K. Kalna, "Scaling/LER study of Si GAA nanowire FET using 3D finite element Monte Carlo simulations," *Solid State Electron.*, vol. 128, pp. 7 – 24, 2017. doi: 10.1016/j.sse.2016.10.018 Extended papers selected from EUROSIOI-ULIS 2016.
- [24] J. Lindberg, M. Aldegunde, D. Nagy, W. G. Dettmer, K. Kalna, A. J. Garcia-Loureiro, and D. Perić, "Quantum Corrections Based on the 2-D Schrödinger Equation for 3-D Finite Element Monte Carlo Simulations of Nanoscaled FinFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 423–429, Feb. 2014. doi: 10.1109/TED.2013.2296209
- [25] D. Nagy, G. Indalecio, A. J. Garca-Loureiro, M. A. Elmessary, K. Kalna, and N. Seoane, "FinFET Versus Gate-All-Around Nanowire FET: Performance, Scaling, and Variability," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 332–340, Feb. 2018. doi: 10.1109/JEDS.2018.2804383
- [26] N. Seoane, G. Indalecio, M. Aldegunde, D. Nagy, M. A. Elmessary, A. J. Garcia-Loureiro, and K. Kalna, "Comparison of Fin-Edge Roughness and Metal Grain Work Function Variability in InGaAs and Si FinFETs," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1209–1216, Mar. 2016. doi: 10.1109/TED.2016.2516921
- [27] S. Bangsaruntip, G. M. Cohen, A. Majumdar, Y. Zhang, S. U. Engelmann, N. C. M. Fuller, L. M. Gignac, S. Mittal, J. S. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M. M. Frank, and J. W. Sleight, "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," in *Proc. IEEE Electron Devices Meeting (IEDM)*, Dec. 2009. doi: 10.1109/IEDM.2009.5424364 pp. 297–300.
- [28] D. Nagy, G. Indalecio, A. J. Garca-Loureiro, M. A. Elmessary, K. Kalna, and N. Seoane, "Metal grain granularity study on a gate-all-around nanowire fet," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 5263–5269, Dec 2017. doi: 10.1109/TED.2017.2764544
- [29] N. Seoane, M. Aldegunde, A. Garcia-Loureiro, R. Valin, and K. Kalna, "3D atomistic simulations of dopant induced variability in nanoscale implant free  $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$  MOSFETs," *Solid State Electron.*, vol. 69, pp. 43 – 49, 2012. doi: 0.1016/j.sse.2011.11.031



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