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# Dynamic Model of Switched-Capacitor DC-DC Converters in the Slow-Switching Limit including Charge Reusing

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## Abstract

An accurate model to analyze the dynamic behavior of two-phase switched-capacitor DC-DC converters in the slow-switching limit regime is proposed taking into account both top and bottom parasitic capacitances as well as the charge reusing approach. This technique features significant improvements in both gain and efficiency with respect to existing solutions. We calculate the slow-switching limit boundary layer taking into account the parasitic capacitances of the flying capacitors and the dynamic and parasitic effects from the switches. The model is highly accurate into this region, featuring better accuracy in both time response and charge consumed than previous models in the literature, as our model takes into account more real phenomena. Also, as we will show it can be used outside this region assuming a certain accuracy loss. The model is verified by experimental results and circuit-level simulations. The model has been implemented in an open-access web simulator, saving up to 10000× in computation time when compared to well-known circuit-level simulators. The applicability of the model is illustrated through the optimization of charge efficiency and time response in a typical situation for light micro-energy harvesting using Dickson, Fibonacci and exponential solutions.

## Index Terms

DC-DC power conversion, switched-capacitor circuits, time-domain analysis, transient response, energy harvesting.

## I. INTRODUCTION

Switched-capacitor DC-DC converters (SCC) are becoming an indispensable component in different applications such as micro-energy harvesting [1], [2], nonvolatile memories [3], [4] or dynamic voltage scaling (DVS) techniques [5], [6]. Classic topologies like Dickson, also called linear (LQP) [7], Fibonacci (FQP) [8] or exponential (EQP) [9] are particular cases of capacitive DC-DC converters, sometimes referred to as charge pumps, that rise up the input voltage, transferring charge packets from the input to a load through a chain of  $N$  capacitors.

The input voltage of the charge pump depends on the particular application. It can be the power supply voltage or the voltage produced by an energy transducer. Also, the kind of load depends on the final purpose of the charge pump. For instance, current-only loads are usual in nonvolatile memories, while purely capacitive loads are common in energy harvesting.

Concerning the charge pump circuit efficiency on integrated circuits, this is severely affected by the parasitic capacitances associated with the flying capacitors, which depend on the manufacturing technology. This efficiency can be improved implementing the charge reusing technique, which was introduced in the 90s [10], [11]. This technique is applied to charge pumps in [12], [13], reaching significant improvements.

In charge pump circuits two operation limits can be distinguished. In the case where the resistive losses are negligible, i.e. the transferring process is completed during each clock phase, the converter operates according to the Slow Switching Limit (SSL). In the case where the resistive losses govern the charge pump behavior, i.e. a constant current flows between capacitors and therefore the transferring process is incomplete during each clock phase, the converter operates in the Fast Switching Limit (FSL). The particular application will dictate the operation regime of the SCC.

Different models to study the performance of the different DC-DC converters have been reported in the literature. Models are preferable to circuit simulations with CAD tools because of their shorter computation time. The simulation time depends on both topology and capacitor values, but simulations which take hours or days with CAD tools can be performed in several minutes with model-based simulators. This work shows that using the model developed in this paper and implemented in MATLAB<sup>®</sup> (available on-line at <http://tec.citius.usc.es/simqp>) allows to save hours or days with respect to circuit-level simulations.

The paper is organized as follows. Section II discusses related work in modeling charge pump circuits. Section III provides a model for capacitive charge pump circuits including top and bottom parasitic capacitances and the charge reusing approach. A study of the operating region of this model is performed in Section IV, and also, the model is validated by circuit-level simulations and experimental results and compared with previous models. In Section V the applicability of the model is demonstrated, illustrating the design process in micro-energy harvesting. Finally, the conclusions of the work are drawn.

## II. RELATED WORK

In this section we present a review of existing charge pump models. We do not intend to review all of them but we will comment on a representative set trying to classify them according to the operation regime, type of charge

pump considered and whether top and bottom parasitic capacitances are taken into account.

Charge pump circuits can be studied in two different regimes, steady-state and transient-state. When a charge pump circuit is studied in the steady-state regime, information about gain, area or efficiency can be extracted. However, a dynamic analysis is essential in certain applications such as energy harvesting, where a time-domain study must be done to estimate the charging time and how much efficiency the energy transducer must provide.

Methods to evaluate the performance of the different **SCC** in the steady-state regime were proposed in [14]–[22]. In [14] a formal study of the theoretical performance of the FQP was realized, showing the maximum ideal attainable output to input voltage ratio, as well as the number of switches required. Through the output impedance of different charge pumps, a performance study in steady-state for SSL and FSL was reported in [15]. An equivalent resistance is calculated in [16] to model the conduction losses in a charge pump at any switching frequency driving a resistive load. A method for calculating the relationship between input and output current, and between input and output voltages in the steady-state regime was illustrated in [17], taking into account the parasitic capacitances and proposing an optimization procedure for the design. In [18] the resistance of the switches was taken into account for the LQP, assuming a constant resistance. This approach permits to optimize the working frequency in steady-state. From the charge balance law (QBL), the authors of [19] obtained the output voltage in steady-state for different charge pumps, including parasitic capacitances. In so doing, the values of the flying capacitors can be optimized and a comparison of the performance of the different charge pump circuits can be made. In [20] a discrete-time numerical method to evaluate the charge pump performance in steady-state can be found. It describes the network of capacitors with matrices and it takes into account the parasitic capacitances. Also, in [21] a method based on a matrix description of the charge pump was used to analyze the FQP, focusing on the impact of parasitic capacitances in steady-state. Finally, a comparison in steady-state of LQP and FQP was presented in [22]. This comparison was realized in the SSL regime and it included the parasitic capacitances of both charge pumps.

All the studies shown above are limited to the steady-state regime despite the fact that a dynamic analysis in the design of a charge pump driving both current and capacitive loads is very useful in practical applications. The related work shown below addresses the topic of dynamic analysis.

In [23] a simple dynamic model of LQP was presented, but it did not take parasitic capacitances into account. In [24] a dynamic analysis of general N-stage LQPs for both current and capacitive loads including bottom parasitic capacitances was reported. Nevertheless, top parasitic capacitances should also be taken into account because they deteriorate the gain of LQP [19], [22] and, consequently, its time response. In [25] a model that includes the top parasitic capacitances for the particular case of LQP was reported. However, this model does not include an expression for the charge consumed by the charge pump. More recently, methodologies to optimize some design parameters based on previous models of LQP have also been published [26].

All the above mentioned work related to dynamic analysis corresponds to the LQP architecture. Because of the structure of this linear topology, a closed-form solution for the rise times can be calculated, but for other topologies like FQP or EQP this is not possible. In [27] a method for performing dynamic analysis of different charge pump circuits in the SSL regime was introduced. The model is then modified to include in FSL the effect of the switches

resistances which are supposed to be constant, resulting in inaccuracies. The model was illustrated for LQP, FQP and EQP without parasitic capacitances. The method gives the output voltage and the accumulated charge after a number of clock cycles.

A circuital model described with average equivalent circuits is developed in [28]. The model is built from the conduction losses. This model is valid for small signal, transient and steady-state conditions ranging from SSL to FSL for SCC which can be described or approximated as first order RC subcircuits. The model is illustrated with both a non-inverting and an inverting 1:1 SCC. In [29] the model is applied to a hybrid converter with a 1:3 SCC. Even though the model is very complete, additional steps are needed to obtain the average equivalent circuit model which represents the dynamic behavior, making the automation for complex topologies harder. Also, parasitic capacitances, which are significant on integrated circuits, are not included in the average circuital model.

In [30] both steady-state and transient behavior of SCC are described by systems of linear equations, applying KVL and the charge conservation law. In this paper all the parasitic resistances of a real implementation are modeled by an equivalent resistance, whose value is calculated in a straightforward manner in SCC topologies where all capacitors are connected in series. Nevertheless, this is not a direct step for more complex topologies or circuits with parasitic capacitances.

In [31] the SCC topologies are modeled through first-order differential equations and applying the charge conservation law, the voltage through all capacitors can be calculated in the SSL regime. In this paper, the authors also introduce a new average loss-based model based on [16], where the conduction losses are modeled by an equivalent resistance. As stated by their authors, the main disadvantages of this model are its very high nonlinear structure and that the accurate estimation of the equivalent resistance may not be an easy task. The model does not include parasitic capacitances either.

Finally, the dynamic model addressed in [32] includes all parasitic capacitances but, as stated by their authors, it is very complex. The reason is that it covers the whole frequency spectrum from SSL to FSL. The complexity of this model makes it hard to reproduce it, as numerical simulations are needed. This model can be reduced to a first-order model, but to do this, the model must be converted to a discrete-time model, which may not be a direct step. Also, through the first-order model it is not possible to have information about the internal dynamics of the converter.

On the other hand, a solution to improve both efficiency and gain of capacitive charge pump circuits was reported in [12], [13]. It consists of charge reusing by adding a clock signal and some switches linking the bottom parasitic capacitances of the charge pumps. To the best of our knowledge, a model that reproduces the dynamic behavior of charge pumps implementing the charge reusing technique has never been previously reported in the literature.

In this paper, we provide an accurate, simple and reproducible model for the transient analysis of any two-phase capacitive charge pump including the charge reusing approach. The model provides both charge and voltage time responses at every flying capacitor and at the output. The model also includes both top and bottom parasitic capacitances and the charge pumps are considered driving both current and capacitive loads. The model is intended for the SSL regime, where the conversion efficiency of charge pumps with parasitic capacitances is maximized

[33]. For this reason, an expression for the determination of the SSL boundary layer will be derived. However, as we will see, it is also possible to use the model outside the SSL regime albeit with a certain accuracy loss. Finally, our model is validated through circuit-level simulations and experimental results, and compared with the main models listed above, decreasing the simulation time and featuring better accuracy with respect to electrical simulations when parasitic capacitances of both the DC-DC converter and the switches are considered.

The main contributions of this paper are: 1) our model accounts for both top and bottom flying parasitic capacitances of DC-DC converters, which leads to better accuracy than the models reported in the literature. Also, we propose and demonstrate that parasitic capacitances from the switches can be included as part of the top and bottom parasitic capacitances, improving the accuracy of the model when the flying capacitors and the switch parasitic capacitances are of the same order; 2) the model is extended to the charge reusing or recycling technique, which might be of interest in low power applications, where the energy efficiency is a design parameter of utter importance, like in micro-energy harvesting, DVS, or Near-Threshold Voltage (NTV) logic; 3) a methodology to design the DC-DC converter outside the SSL regime is proposed consisting of finding the SSL boundary layer in a given design space with a given error level when compared to the results from a circuit-level simulator. The paper illustrates this methodology for the switching frequency-switching transistor width parameter space of any SCC; 4) we illustrate all the above with the design of a DC-DC converter for micro-energy harvesting constraints, showing the trade-off between time response and charge efficiency; and 5) a web simulator of the proposed model has been developed that significantly shortens the computation time with respect to circuit-level simulators [34].

### III. DYNAMIC MODEL

This section addresses the model for the transient analysis of any capacitive charge pump driving current or capacitive loads in the SSL regime. Section III-A introduces the model with parasitic capacitances. Section III-B extends the model for charge pumps with charge reusing. To the best of our knowledge, none of these two approaches have been previously reported in the literature. Our model is based on the one reported in [27], which is demonstrated for any topology of two-phase capacitive charge pumps driving current or capacitive loads in the SSL regime. However, the model in [27] was not illustrated for charge pumps with parasitic capacitances. For the sake of clarity and without loss of generality we will illustrate our model for a 2-stage Dickson charge pump. In Appendix B the model is extended to two other well-known DC-DC converters, i.e., the FQP and the EQP topologies.

Fig. 1 displays the schematics of LQP with  $3\times$  gain (LQP3 $\times$ ) driving a capacitance load ( $C_s$ ) and a current load ( $I_{out}$ ) with an input voltage  $V_{in}$ .  $\alpha C_j$  and  $\beta C_j$  are the bottom and top parasitic capacitances of the capacitors of the charge pump. Typically  $\alpha = 0.1$  and  $\beta = 0.05$  on integrated circuits. These will be the values considered throughout the paper unless stated otherwise. Fig. 2 shows a timing diagram for a charge pump, like LQP, controlled by two non-overlapping clock signals,  $clk1$  and  $clk2$ . In Section III-B, the model for the charge reusing approach will be developed, which needs an additional switch driven by a third clock signal  $clk3$ . This is a very short signal between  $clk1$  and  $clk2$ , therefore we will assume that the waveforms of these two latter signals do not change when  $clk3$  is introduced.

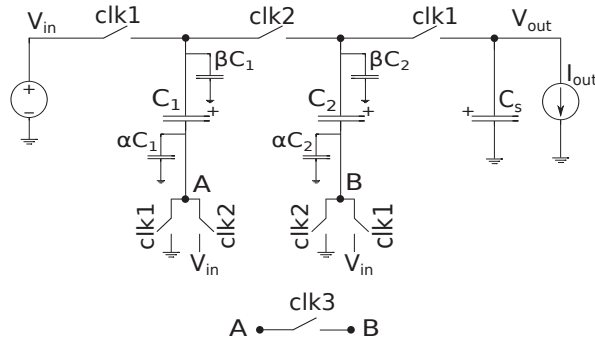


Fig. 1. Schematic of a 2-stage Dickson charge pump (LQP3 $\times$ ) with clock signals  $clk1$  and  $clk2$ . The third clock signal,  $clk3$ , is used in the charge reusing approach.

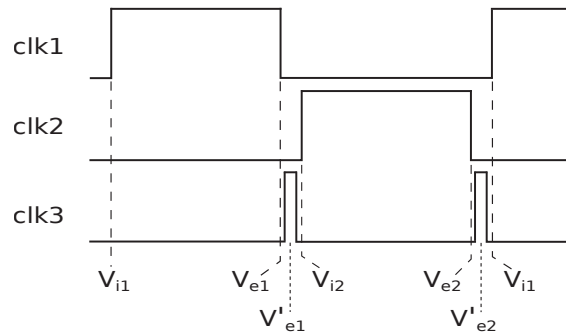


Fig. 2. Timing diagram with  $clk1$  and  $clk2$  clock signals for a standard charge pump.  $clk1$ ,  $clk2$  and  $clk3$  are used in the charge reusing approach. The  $V$  variables refer to the voltage across each capacitor.

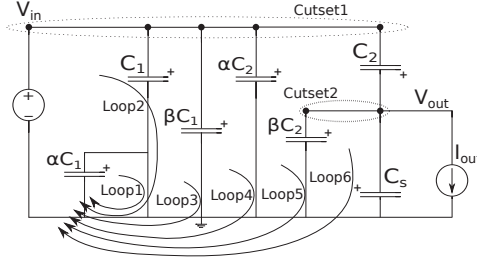
### A. Model with parasitic capacitances

The charge and voltage in the SSL regime at every node can be determined by KVL and KCL for every  $clk1$  and  $clk2$  cycle. In a general situation, this yields  $3N+2$  equations for a charge pump with  $N$  capacitors, which can be expressed in matrix formulation.

Analyzing the particular case of the LQP3 $\times$  shown in Fig. 1, first we will consider the situation with  $clk1$  high, shown in Fig. 3. KVL gives (1)–(6) for *Loop1* through *Loop6* in Fig. 3. KCL provides (7) and (8). The former corresponds to *Cutset1*, while the latter is for *Cutset2*.  $V_{i1}(V_{in})$  and  $V_{i1}(C_j)$  represent the input voltage  $V_{in}$  and the voltage at the rising edge of  $clk1$  at a given capacitor  $C_j$ , respectively, as Fig.2 shows.  $Q_1(V_{in})$  and  $Q_1(C_j)$  refer to the net charge provided through  $V_{in}$  and the net charge flowing into the capacitor under study, respectively, during  $clk1$  high.

$$0 = V_{i1}(\alpha C_1) + \frac{Q_1(\alpha C_1)}{\alpha C_1} \quad (1)$$

$$V_{i1}(V_{in}) = V_{i1}(C_1) + \frac{Q_1(C_1)}{C_1} \quad (2)$$


 Fig. 3. Dickson charge pump with 3 $\times$  gain (LQP3 $\times$ ) with  $ckl$  high.

$$V_{i1}(V_{in}) = V_{i1}(\beta C_1) + \frac{Q_1(\beta C_1)}{\beta C_1} \quad (3)$$

$$V_{i1}(V_{in}) = V_{i1}(\alpha C_2) + \frac{Q_1(\alpha C_2)}{\alpha C_2} \quad (4)$$

$$V_{i1}(V_{in}) + V_{i1}(C_2) + \frac{Q_1(C_2)}{C_2} = V_{i1}(\beta C_2) + \frac{Q_1(\beta C_2)}{\beta C_2} \quad (5)$$

$$V_{i1}(V_{in}) + V_{i1}(C_2) + \frac{Q_1(C_2)}{C_2} = V_{i1}(C_s) + \frac{Q_1(C_s)}{C_s} \quad (6)$$

$$Q_1(V_{in}) + Q_1(C_2) = Q_1(C_1) + Q_1(\beta C_1) + Q_1(\alpha C_2) \quad (7)$$

$$0 = Q_1(C_2) + Q_1(\beta C_2) + Q_1(C_s) + I_{out}TD \quad (8)$$

Equations (1)–(8) can be expressed in matrix formulation through (9), with  $\mathbf{A}_1$  and  $\mathbf{B}_1$  given in (10) and (11).  $\mathbf{V}_{i1}$  is a column vector whose elements are  $V_{i1}(V_{in})$  and  $V_{i1}(C_j)$ , and  $\mathbf{Q}_1$  is a column vector whose elements are  $Q_1(V_{in})$  and  $Q_1(C_j)$ . Both matrices are listed in Appendix A.  $\mathbf{K}_1$  is a column vector that takes into account the effect of the current load,  $I_{out}$ . It is given by (12), where  $D$  is the clock duty cycle and  $T$  the clock period.

$$\mathbf{A}_1 \mathbf{Q}_1 + \mathbf{B}_1 \mathbf{V}_{i1} = \mathbf{K}_1 \quad (9)$$

$$\mathbf{A}_1 = \begin{pmatrix} 0 & \frac{-1}{\alpha C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{\beta C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{\alpha C_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_2} & \frac{-1}{\beta C_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_2} & 0 & \frac{-1}{C_s} \\ 1 & 0 & -1 & -1 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & -1 & -1 \end{pmatrix} \quad (10)$$



$$\mathbf{B}_2 = \begin{pmatrix} 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & -1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix} \quad (15)$$

$$\mathbf{K}_2 = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_{out}T(1-D) \end{pmatrix}^t \quad (16)$$

Through (17) and (18), the two matrices that represent the voltage at all elements at the falling edge of  $clk1$  and  $clk2$ ,  $\mathbf{V}_{e1}$  and  $\mathbf{V}_{e2}$  respectively, are found. Both matrices are listed in Appendix A. The charge consumed by each capacitor,  $\mathbf{Q}_1$  and  $\mathbf{Q}_2$ , is calculated through (9) and (13).

$$\mathbf{V}_{e1} = \mathbf{V}_{i1} + \mathbf{CQ}_1 \quad (17)$$

$$\mathbf{V}_{e2} = \mathbf{V}_{i2} + \mathbf{CQ}_2 \quad (18)$$

Similarly to the procedure followed in [27], where  $\mathbf{V}_{e1} = \mathbf{V}_{i2}$  and  $\mathbf{V}_{e2} = \mathbf{V}_{i1}$  is supposed, after some basic operations the voltages across the capacitors at the end of the  $m$ th cycle ( $V_{o,m}(V_{in})$  or  $V_{o,m}(C_j)$ ) are found:

$$\mathbf{V}_{o,m} = \mathbf{P}^m \mathbf{V}_i + \sum_{k=0}^{m-1} \mathbf{P}^k (\mathbf{W}_1 \mathbf{K}_1 + \mathbf{W}_2 \mathbf{K}_2) \quad (19)$$

where  $\mathbf{V}_i$  is the initial voltage across each capacitor at  $t = 0$  ( $m = 0$ ) and  $\mathbf{P}$ ,  $\mathbf{W}_1$  and  $\mathbf{W}_2$  resulting from operations with matrices  $\mathbf{A}_1$ ,  $\mathbf{B}_1$ ,  $\mathbf{A}_2$  and  $\mathbf{B}_2$ . The expressions for  $\mathbf{P}$ ,  $\mathbf{W}_1$  and  $\mathbf{W}_2$  are listed in Appendix A.

The accumulated charge at the end of the  $m$ th clock cycle is found with a similar procedure:

$$\begin{aligned} \mathbf{Q}_{acc,m} = & \mathbf{M} \sum_{p=0}^{m-1} \mathbf{P}^p \mathbf{V}_i + \left[ \mathbf{M} \sum_{p=1}^{m-1} \sum_{q=0}^{p-1} \mathbf{P}^q \mathbf{W}_1 + m \mathbf{N}_1 \right] \mathbf{K}_1 \\ & + \left[ \mathbf{M} \sum_{p=1}^{m-1} \sum_{q=0}^{p-1} \mathbf{P}^q \mathbf{W}_2 + m \mathbf{N}_2 \right] \mathbf{K}_2 \end{aligned} \quad (20)$$

with  $\mathbf{M}$ ,  $\mathbf{N}_1$  and  $\mathbf{N}_2$  resulting from operations with matrices  $\mathbf{A}_1$ ,  $\mathbf{B}_1$ ,  $\mathbf{A}_2$  and  $\mathbf{B}_2$ . The expressions for  $\mathbf{M}$ ,  $\mathbf{N}_1$  and  $\mathbf{N}_2$  can be found in Appendix A.

### B. Model with charge reusing technique

Parasitic capacitances cause charge wasted during the circuit operation and the gain of the charge pump is decreased. The charge reusing technique leads to higher gain and better charge or energy efficiency [13].

The charge reusing technique links all bottom parasitic capacitances between the falling edge of  $clk1$  and the rising edge of  $clk2$ , and between the falling edge of  $clk2$  and the rising edge of  $clk1$ , as Fig. 1 and Fig. 2 show. In so doing, the voltage across the capacitors at the falling edge of  $clk1$ ,  $\mathbf{V}_{e1}$ , is not longer the same as that at the

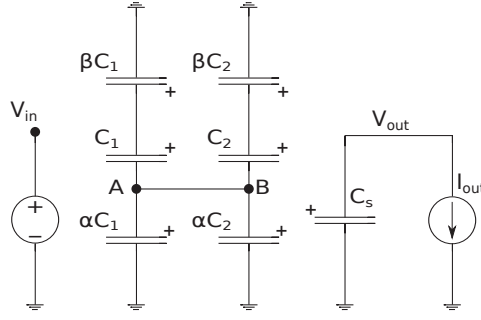


Fig. 5. Dickson charge pump with  $3\times$  gain (LQP $3\times$ ) with  $clk3$  high implementing the charge reusing technique.

rising edge of  $clk2$ ,  $V_{i2}$ , because a third non-overlapping clock signal,  $clk3$ , drives the additional switches that link some bottom parasitic capacitances (see Fig. 2 and Fig. 5). During  $clk3$ ,  $V_{e1}$  changes to an intermediate voltage  $V'_{e1}$ , being  $V_{i2} = V'_{e1}$ . Similarly, at the start of the next cycle,  $V_{i1} = V'_{e2}$ . This is an iterative process across the clock cycles of the transient time of the charge pump. Inserting these new values for  $V_{i2}$  and  $V_{i1}$  in the procedure to obtain (19) and (20), the voltages across the capacitors and the charge consumed at the end of the  $m$ th cycle are found.

Algorithm 1 conveys a summary of the main steps of this procedure for LQP $3\times$ . This procedure would be the same for more stages or for any other capacitive DC-DC converter topology. If charge reusing is considered after the falling edge of  $clk1$ , the charge flows between nodes A and B until their voltages equal each other. For LQP under this situation, the voltage at node A is grounded and the voltage at node B is  $V_{in}$  at the start of  $clk3$ . This can be expressed as the voltage across the bottom parasitic capacitances  $V_{e1}(\alpha C_{jA}) = 0$  and  $V_{e1}(\alpha C_{jB}) = V_{in}$ , respectively. Therefore, (21) and (22) can be calculated at the end of  $clk3$  for a charge pump with  $N$  stages, where the floor function  $\lfloor x \rfloor$  is the largest integer not greater than  $x$ . We assume the same size for all capacitors  $C_j$  in LQP, but for other topologies,  $C_j$  should be appropriately sized [19]. It should be noted that  $V_{e1}(\alpha C_{jA}) = V_{e1}(\alpha C_1)$  and  $V_{e1}(\alpha C_{jB}) = V_{e1}(\alpha C_2)$  for LQP $3\times$  as Fig. 5 shows.

$$V'_{e1}(\alpha C_{jA}) = \frac{V_{e1}(\alpha C_{jB}) \lfloor \frac{N}{2} \rfloor}{N} \quad (21)$$

$$V'_{e1}(\alpha C_{jB}) = \frac{V_{e1}(\alpha C_{jA}) \lfloor \frac{N}{2} \rfloor}{N} \quad (22)$$

To calculate the voltage across the top parasitic capacitances,  $V'_{e1}(\beta C_j)$ , the charge balance law (QBL) that states that in a system of capacitors, the net sum of all charges in a node at any instance of the charge transfer is equal to zero, should be applied. This law can be expressed by (23), in which the charge in  $C_j$  and  $\beta C_j$  just after the falling edge of  $clk1$ ,  $Q$ , is equal to the charge just before the rising edge of  $clk2$ ,  $Q'$ .

$$Q(C_j) + Q(\beta C_j) = Q'(C_j) + Q'(\beta C_j) \quad (23)$$

From (23),  $V'_{e1}(\beta C_j)$  can be calculated as:

$$V'_{e1}(\beta C_j) = \frac{C_j[V_{e1}(\beta C_j) - V_{e1}(\alpha C_j)] + \beta C_j V_{e1}(\beta C_j) + C_j V'_{e1}(\alpha C_j)}{C_j + \beta C_j} \quad (24)$$

Finally through (25), we have  $V'_{e1}(C_j)$ ,

$$V'_{e1}(C_j) = V'_{e1}(\beta C_j) - V'_{e1}(\alpha C_j) \quad (25)$$

Similarly,  $V'_{e2}$  can be obtained after the falling edge of  $clk2$ . For LQP under this situation, at the start of  $clk3$  the voltage at nodes A and B is  $V_{in}$  and ground respectively, yielding

$$V'_{e2}(C_j) = V'_{e2}(\beta C_j) - V'_{e2}(\alpha C_j) \quad (26)$$

where

$$V'_{e2}(\alpha C_{jA}) = \frac{V_{e1}(\alpha C_{jA}) \lceil \frac{N}{2} \rceil}{N} \quad (27)$$

$$V'_{e2}(\alpha C_{jB}) = \frac{V_{e1}(\alpha C_{jA}) \lceil \frac{N}{2} \rceil}{N} \quad (28)$$

$$V'_{e2}(\beta C_j) = \frac{C_j[V_{e2}(\beta C_j) - V_{e2}(\alpha C_j)] + \beta C_j V_{e2}(\beta C_j) + C_j V'_{e2}(\alpha C_j)}{C_j + \beta C_j} \quad (29)$$

with the ceiling function  $\lceil x \rceil$  being the smallest integer not less than  $x$ .

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**Algorithm 1** Pseudocode to calculate  $V'_{e1}$  and  $V'_{e2}$  in LQP3 $\times$  when charge reusing is considered

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- 1: **if** between falling edge of  $clk1$  and rising edge of  $clk2$  **then**
  - 2:      $V'_{e1}(\alpha C_1) = \frac{V_{e1}(\alpha C_2)}{2}$
  - 3:      $V'_{e1}(\beta C_1) \leftarrow$  QBL
  - 4:      $V'_{e1}(C_1) = V'_{e1}(\beta C_1) - V'_{e1}(\alpha C_1)$
  - 5:      $V'_{e1}(\alpha C_2) = \frac{V_{e1}(\alpha C_2)}{2}$
  - 6:      $V'_{e1}(\beta C_2) \leftarrow$  QBL
  - 7:      $V'_{e1}(C_2) = V'_{e1}(\beta C_2) - V'_{e1}(\alpha C_2)$
  - 8: **else if** between falling edge of  $clk2$  and rising edge of  $clk1$  **then**
  - 9:      $V'_{e2}(\alpha C_1) = \frac{V_{e2}(\alpha C_1)}{2}$
  - 10:      $V'_{e2}(\beta C_1) \leftarrow$  QBL
  - 11:      $V'_{e2}(C_1) = V'_{e2}(\beta C_1) - V'_{e2}(\alpha C_1)$
  - 12:      $V'_{e2}(\alpha C_2) = \frac{V_{e2}(\alpha C_1)}{2}$
  - 13:      $V'_{e2}(\beta C_2) \leftarrow$  QBL
  - 14:      $V'_{e2}(C_2) = V'_{e2}(\beta C_2) - V'_{e2}(\alpha C_2)$
  - 15: **end if**
-

TABLE I  
SIMULATION TIME COMPARISON

Topology	Circuit-level simulator		This work
	Ideal switch	Transmission gate	
LQP8x	3.07 h	6.04 days	1.91 min
FQP8x	4.55 h	13.80 days	2.12 min
EQP8X	4.33 h	10.69 days	1.47 min

#### IV. MODEL ANALYSIS

This section addresses an analysis of the accuracy of our model. The first subsection describes the implementation of the model in a matrix-based language. The second subsection presents the application range where our model has high accuracy. Finally, the third subsection introduces a comparison between the results with our model and both experimental measurements and circuit-level simulations and with other models in the literature.

##### A. Model Implementation

The model introduced in Section III including parasitic capacitances with and without charge reusing has been implemented for any number of stages in a matrix-based language, MATLAB<sup>®</sup>, yielding fast results. Based on this implementation, we built a user-friendly open-access simulator available at [34]. The results shown in the next sections are from this simulator.

Table I compares the simulation time for different charge pumps from a widely used circuit-level simulator using both ideal switches and transmission gates and those of our simulator. To run the simulations an Intel<sup>®</sup> Xeon CPU E5-2637 v2 at 3.5 GHz with 64 Gb RAM was used. The data shown correspond to a switching frequency of 250 kHz and a  $C_s/C_t$  ratio of  $10^4$ , where  $C_t$  is the sum of the flying capacitors. As seen, the computation time savings using our model are very large, especially when the charge pump features transmission gates. The model is up to  $175\times$  faster than circuit-level simulations with ideal switches and up to  $10000\times$  faster when real switches are considered.

##### B. Application Range

The model developed in this paper is based on the assumption that the capacitors are fully charged during each clock phase, i.e. the charge pump works in the SSL regime. Fig. 6 shows the current on a flying capacitor of an LQP at different clock frequencies, being this behavior similar for all capacitive charge pump circuits. Fig. 6(a) shows the case when the current at the end of each clock cycle is zero. This means that the capacitor is fully charged and the charge pump works in the SSL regime. In Fig. 6(b) the current at the end of each clock cycle is near zero, therefore the charge pump works in the limit of SSL mode. In these two cases, simulation results from our model match circuit-level simulations very accurately. Finally, in Fig. 6(c) the flying capacitor is not fully charged because the current is not zero at the end of each clock cycle and the charge pump operates outside the SSL regime. Under

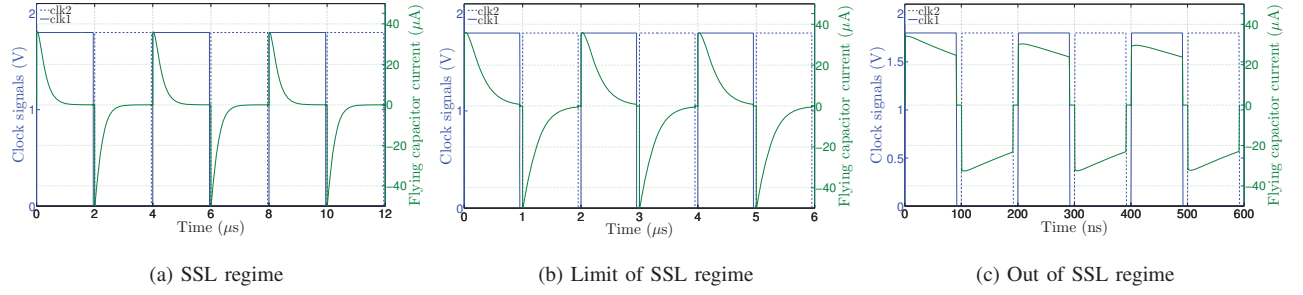


Fig. 6. Different work regimes for capacitive charge pumps.

this condition our model presents a loss of accuracy whose magnitude depends on the charge level of the flying capacitors. Next, we will derive an expression to quantify the boundary layer of the SSL operating region.

To ensure that the capacitive charge pump works in the SSL regime, where applications such as low power consumption or energy harvesting are designed because the conversion efficiency **is generally maximized in presence of parasitic capacitances** [33], (30) extracted from [27] can be applied,

$$f < \frac{1}{10 R_{total} C_{total}} \quad (30)$$

being  $R_{total}$  the sum of the on-resistance of the switches and the Equivalent Series Resistance (ESR) of the capacitors, and  $C_{total}$  the sum of the capacitance of the largest flying capacitor ( $C_j$ ) with its parasitic capacitances ( $\alpha C_j$  and  $\beta C_j$ ) and the parasitic capacitances from the switches ( $C_{sw}$ ).

If the switches are implemented with transmission gates, the on-resistance depends on the working region of the transistors. The worst case can be estimated as the resistance of the PMOS transistor with  $V_{DS} = 0$  through (31),

$$r_{onPMOS} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{DD} - |V_{TH}| - \frac{1}{2} (V_{DD} - V_{DS}))} \quad (31)$$

where  $\mu$  is the hole mobility,  $C_{ox}$  the capacitance per unit gate area of the oxide layer,  $W$  and  $L$  the gate width and length of the PMOS transistor, respectively,  $V_{DD}$  the supply voltage,  $V_{TH}$  the threshold voltage and  $V_{DS}$  the drain-source voltage. Therefore, assuming that the ESR of the flying capacitors is negligible,  $R_{total}$  can be taken approximately equal to  $r_{onPMOS}$ . Also, for the same operating conditions of the transistors, the parasitic capacitance of a transmission gate can be estimated through (32),

$$C_{sw} = C_{ox} W L \quad (32)$$

Finally from (30), (31) and (32), the limit of the SSL regime for a specific technology of any capacitive charge pump circuit can be calculated through (33) as,

$$f < \frac{1}{10 r_{onPMOS} (C_j + \alpha C_j + \beta C_j + C_{sw})} \quad (33)$$

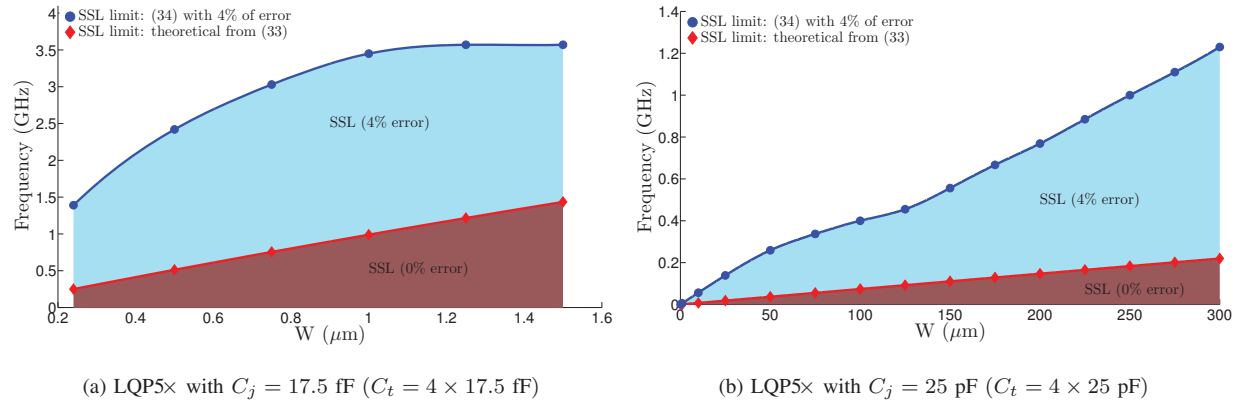


Fig. 7. Limit of SSL regime: theoretical from (33), and measured assuming 4% error.

(33) sets the boundary layer of the SSL working region, where the model is highly accurate. Nevertheless, it is also possible to apply our model beyond this region assuming a certain error level with respect to the outcome of a circuit-level simulator. The error level is calculated through (34),

$$error (\%) = \frac{|(G_{mod} - 1) - (G_{sim} - 1)|}{G_{mod} - 1} \times 100 \quad (34)$$

with  $G_{mod}$  being the gain from our model, and  $G_{sim}$  the one from the circuit-level simulator.

Fig. 7 plots with a solid-line with dots the 0% error SSL boundary layer and the one corresponding to a 4% error in the design space given by the switching frequency,  $f$ , and the width of the transmission gate,  $W$ , for an LQP5x on an integrated circuit in standard  $0.18 \mu\text{m}$  CMOS technology under the conditions of low and large  $C_j$ . In both cases we have set  $L = 180$  nm. As apparent, this study can be extended to other charge pump topologies. The area below these two curves are the regions where the switching frequency and the width of the transmission gates guarantee SSL operation with either zero or up to 4% error levels. As expected, the SSL region changes meaningfully with the flying capacitor values. The shape of the curve is difficult to predict because of the different regions of operation of the switches, and the inherent nonlinearity of parameters like the transmission gate resistances and parasitic capacitances.

Parasitic capacitances from the switches,  $C_{sw}$ , as well as dynamic effects such as charge injection and feedthrough affect the gain when  $C_{sw} \approx C_j$ . In practice, it is hard to isolate these two effects through simulation. Both effects, however, can be accounted for by introducing two new parameters,  $\alpha_{eff}$  and  $\beta_{eff}$ , as the effective  $\alpha$  and  $\beta$  values. To obtain these values, a trial-and-error comparison between our model and a circuit-level simulation is needed, as it is not possible to extract an equation to calculate the exact value for  $C_{sw}$  because this capacitance changes with the operating region of the switches. Thus,  $\alpha_{eff}$  and  $\beta_{eff}$  act as fitting parameters between circuit-level simulations and our model, and they replace  $\alpha$  and  $\beta$ . This procedure includes the leakage currents in  $\alpha_{eff}$  and  $\beta_{eff}$ . After the iterative process to find  $\alpha_{eff}$  and  $\beta_{eff}$ , we can estimate capacitances  $C_{sw_{eff,\alpha}}$  and  $C_{sw_{eff,\beta}}$  through (35) and (36).  $C_{sw_{eff,\alpha}}$  and  $C_{sw_{eff,\beta}}$  are not actual capacitances in the circuit but they are introduced to include the global effect of

TABLE II  
EFFECTIVE  $C_{sw}$  FOR LQP5× WITH  $C_j = 17.5$  fF IN STANDARD 0.18  $\mu\text{m}$  CMOS TECHNOLOGY

W ( $\mu\text{m}$ )	$C_j = 17.5$ fF ( $\alpha = 0.1, \beta = 0.05$ )			
	$C_{sw_{\text{eff},\alpha}}$ (fF)	$C_{sw_{\text{eff},\beta}}$ (fF)	$\alpha_{\text{eff}}$	$\beta_{\text{eff}}$
0.24	5.73	7.17	0.1819	0.1524
0.5	10.19	12.37	0.2455	0.2267
0.75	14.45	17.17	0.3065	0.2953
1	18.58	21.97	0.3654	0.3639
1.25	22.61	26.49	0.4230	0.4285
1.5	26.47	31.15	0.4781	0.4950

the capacitances from all the switches in the charge pump, as well as all the dynamic effects (charge injection and feedthrough) and all the leakage currents.

$$C_{sw_{\text{eff},\alpha}} = (\alpha_{\text{eff}} - \alpha) C_j \quad (35)$$

$$C_{sw_{\text{eff},\beta}} = (\beta_{\text{eff}} - \beta) C_j \quad (36)$$

We have found that, for each topology, these effective capacitances only depend on the number of stages and the dimension of the switches. Therefore, once these global effective capacitances are determined for a particular number of stages and dimensions of the switches, our model can be used to study the effect of changing  $C_j$ ,  $\alpha$  or  $\beta$ , with the new  $\alpha_{\text{eff}}(\alpha, C_j)$  and  $\beta_{\text{eff}}(\beta, C_j)$  calculated through (37) and (38) from the  $C_{sw_{\text{eff},\alpha}}$  and  $C_{sw_{\text{eff},\beta}}$  for those particular conditions.

$$\alpha_{\text{eff}}(\alpha, C_j) = \alpha + \frac{C_{sw_{\text{eff},\alpha}}}{C_j} \quad (37)$$

$$\beta_{\text{eff}}(\beta, C_j) = \beta + \frac{C_{sw_{\text{eff},\beta}}}{C_j} \quad (38)$$

As an example, Table II and Table III summarize the values for  $C_{sw_{\text{eff},\alpha}}$  and  $C_{sw_{\text{eff},\beta}}$  as well as  $\alpha_{\text{eff}}$  and  $\beta_{\text{eff}}$  for the different gate widths depicted in Fig. 7(a) and Fig. 7(b) respectively. In the situation in Fig. 7(a), the gain of the charge pump is severely affected by  $C_{sw_{\text{eff}}}$  since  $C_{sw_{\text{eff}}} \approx C_j$ , so  $\alpha_{\text{eff}} \gg \alpha$  and  $\beta_{\text{eff}} \gg \beta$  even for low  $W$  values as can be seen in Table II. However, when  $C_{sw_{\text{eff}}} \ll C_j$ , Table III,  $\alpha_{\text{eff}} \approx \alpha$  and  $\beta_{\text{eff}} \approx \beta$  and the effect of the switches can be neglected with only small corrections for large  $W$ .

Finally, Table IV collects frequency and gate widths of different applications found in the literature that work in the SSL regime. It should be noted that although Dynamic Voltage Frequency Scaling (DVFS) and NTV designs employ step-down capacitive DC-DC converters, our model would still be valid in these cases, as it is based on KCL and KVL.

TABLE III  
EFFECTIVE  $C_{sw}$  FOR LQP5X WITH  $C_j = 25$  pF IN STANDARD 0.18  $\mu\text{m}$  CMOS TECHNOLOGY

W ( $\mu\text{m}$ )	$C_j = 25$ pF ( $\alpha = 0.1, \beta = 0.05$ )			
	$C_{sw\text{eff},\alpha}$ (pF)	$C_{sw\text{eff},\beta}$ (pF)	$\alpha_{\text{eff}}$	$\beta_{\text{eff}}$
0.24	$5.73 \times 10^{-3}$	$7.17 \times 10^{-3}$	0.1	0.05
1	$18.58 \times 10^{-3}$	$21.97 \times 10^{-3}$	0.1	0.05
10	$83.40 \times 10^{-3}$	0.15	0.1	0.05152
25	0.14	0.48	0.1014	0.05481
50	0.35	1.04	0.1035	0.06037
75	0.55	1.61	0.1055	0.06609
100	0.74	2.19	0.1074	0.07193
125	0.94	2.79	0.1094	0.07791
150	1.11	3.40	0.1111	0.08402
175	1.27	4.02	0.1127	0.09021
200	1.44	4.65	0.1144	0.09646
225	1.60	5.27	0.1160	0.10275
250	1.79	5.90	0.1179	0.10901
275	1.96	6.53	0.1196	0.11527
300	2.14	7.15	0.1214	0.12147

TABLE IV  
DC-DC CONVERTER APPLICATIONS IN THE SSL REGIME

	Energy Harvesting [35], [36]	Flash Memories [18]	DVFS, NTV [37]–[40]
Frequency	< 1 MHz	$\sim 50$ MHz	100-700 MHz
Gate Width	$\sim 500$ nm	$> 25$ $\mu\text{m}$	$> 50$ $\mu\text{m}$
$C_j$	$\sim 10$ pF	$\sim 50$ pF	$\sim 100$ pF

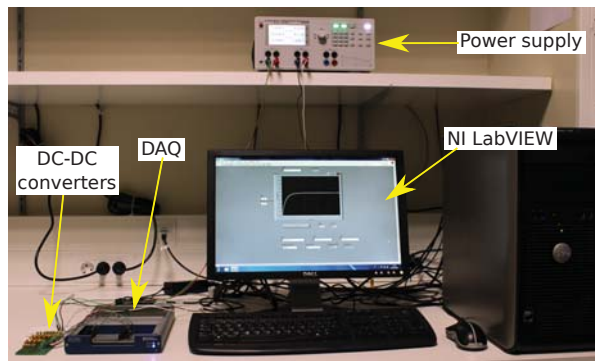


Fig. 8. Experimental set-up for the validation of our model.

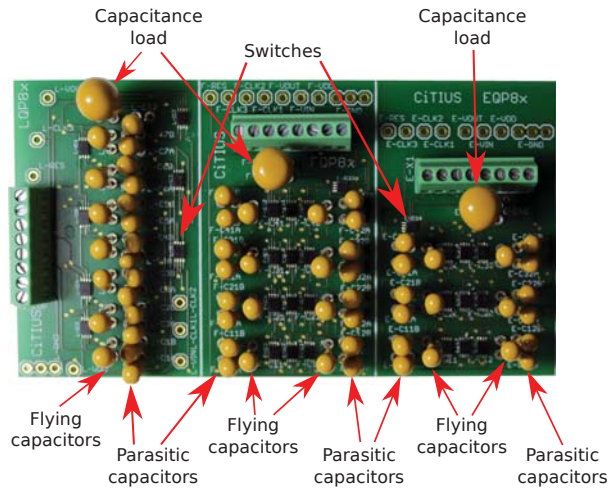


Fig. 9. PCB with DC-DC converters LQP8 $\times$ , FQP8 $\times$  and EQP8 $\times$  with and without charge reusing.

### C. Model Validation

In this subsection and without loss of generality the model is validated with both experimental results and circuit-level simulations for the minimum common gain of the three main topologies of capacitive DC-DC converters, that is, LQP8 $\times$ , FQP8 $\times$  and EQP8 $\times$ . Also, we compare our models with dynamic models found in the literature [23], [24], [27]. The comparison with the model addressed in [28]–[32] is not straightforward. Obtaining simulation data with such models for complex topologies like FQP8 $\times$  or EQP8 $\times$  with parasitic capacitances would be a very lengthy process, exceeding the scope of this paper.

With respect to the model addressed in [23] and [24], it is intended for LQP and it does not account for current load nor for top parasitic capacitances. Therefore, it is only applicable to purely capacitive loads with bottom parasitic capacitances. For the sake of clarity, the model is reproduced in (39) and (40), where  $V_{out}$  is the output voltage in the load capacitor  $C_s$ ,  $t_{target}$  is the time needed to reach a given output voltage,  $N$  the number of stages,  $C$  the flying capacitors,  $V_{out}(0)$  the output voltage at  $t = 0$ ,  $V_{out}(t_{target})$  the output voltage at  $t = t_{target}$  and  $Q$  the charge consumed from  $t = 0$  to  $t_{target}$ .

$$t_{target} = T \left( N \frac{C_s}{C} + 0.3N + 0.6 \right) \ln \left[ \frac{(N+1)V_{DD} - V_{out}(0)}{(N+1)V_{DD} - V_{out}(t_{target})} \right] \quad (39)$$

$$Q = (N + 1) \left( \frac{C_t}{3} + C_s \right) [V_{out}(t_{target}) - V_{out}(0)] + \alpha C_t V_{DD} \frac{t_{target}}{T} \quad (40)$$

As said above, the model introduced in [27] **does not account for parasitic capacitances and charge reusing.**

The experimental set-up for our model validation is shown in Fig. 8. It comprises a Data Acquisition (DAQ) board with NI LabVIEW to both provide the clock signals for the DC-DC converters and make the measurements. The DC-DC converters are laid down in a Printed Circuit Board (PCB), as Fig. 9 shows. The DC-DC converters are implemented with tantalum capacitors with nominal values  $C_j = 1 \mu\text{F}$  with 20% of tolerance, and with circuits

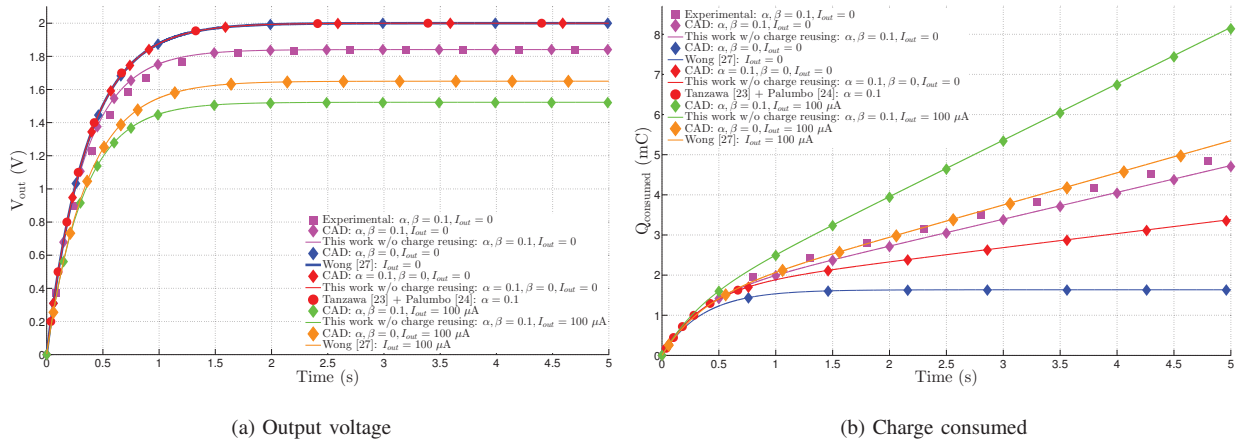


Fig. 10. Comparison of the model in this paper, circuit-level simulations and other models in the literature for the dynamic response of LQP8x.

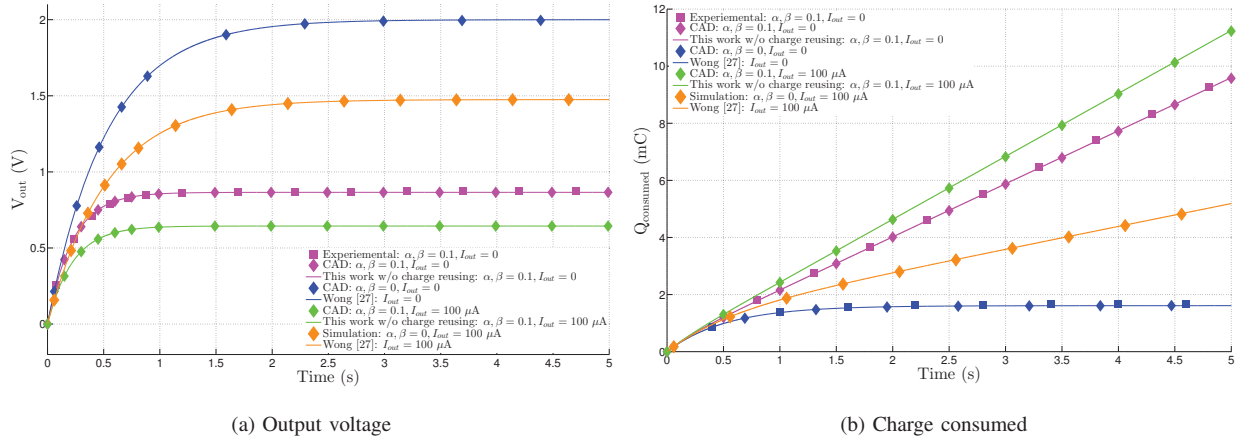


Fig. 11. Comparison of the model in this paper, circuit-level simulations and other models in the literature for the dynamic response of EQP8x.

TS5A23166 as switches ( $R_{on} = 0.9 \Omega$ ). Top and bottom parasitic capacitances to reproduce actual conditions of an integrated circuit were included with tantalum capacitors of the same series with nominal values  $\alpha C_j, \beta C_j = 100 \text{ nF}$ , which means  $\alpha, \beta = 0.1$ . With these data, according to (33),  $f_L = 90 \text{ kHz}$  is the limit frequency for the DC-DC converters to be within the SSL regime. In our experimental set-up we have chosen a clock period  $T = 500 \mu\text{s}$  with a pulse width of  $235 \mu\text{s}$  for  $clk1$  and  $clk2$ . The period of signal  $clk3$ , which provides charge reusing, is set at  $T = 250 \mu\text{s}$  with a pulse width of  $14.25 \mu\text{s}$ , enough to complete the charge distribution between the corresponding nodes in the charge pump under study. The input voltage is set to  $V_{in} = 0.25 \text{ V}$ . Thus, for the three charge pumps the ideal output voltage at  $t \rightarrow \infty$  is  $V_{out} = 2 \text{ V}$  with gain  $G = 8$ . The output capacitor is also a tantalum capacitor, whose size is chosen as  $C_s = 100 \mu\text{F}$ . Fig. 10 - Fig. 12 convey results for several static current loads, while Fig. 13 gathers transient results with dynamic current loads.

Voltages are directly measured through the DAQ system. The charge drawn from the input voltage source is

indirectly measured through a  $1.9\ \Omega$  resistor placed in the input of the charge pumps, integrating its current along time. This resistor does not affect the charge pump behavior because the measurements are made in the SSL regime.

Circuit-level simulations have been performed for a standard  $0.18\ \mu\text{m}$  CMOS technology with switches sized at  $W = 100\ \mu\text{m}$  and  $L = 180\ \text{nm}$  to yield the same behavior as that of the switches of the experimental setup. Flying and parasitic capacitors have been set to the same values as those of the experimental set-up.

Fig. 10(a)–(b) show the comparison of the time response for LQP8 $\times$  without charge reusing for our model and the models in [23], [24] and [27]. The output voltage is studied for a capacitive-only load,  $I_{out} = 0$ , and for both current and capacitive loads,  $I_{out} \neq 0$ . As seen, the model in [23] and [24] underestimates the time response and overestimates the gain because it does not include the parasitic capacitances, as it can be seen in (39). The same happens to the model in [27]. It should be noted that only the top parasitic capacitances affect the gain and the time response. As said above, the expected gain is  $8\times$ , yielding  $V_{out} = 2\ \text{V}$ . Nevertheless, the actual gain is  $7.36\times$ , leading to  $V_{out} = 1.84\ \text{V}$  in steady state. Finally, for LQP with  $I_{out} = 100\ \mu\text{A}$  in Fig. 10(a), the gain is greatly affected by the current load, changing from  $7.36\times$  for a purely capacitive load to  $6.09\times$  for a current load. Also, for the actual situation the gain predicted by [27] drops from  $6.60\times$  to  $6.09\times$ .

Concerning charge, when parasitic capacitances are not taken into account as in [27], Fig. 10(b), the charge consumption in the steady state is wrongly estimated to be null for charge pumps with purely capacitive loads. However, when accounting for parasitic capacitances the actual situation is that their charge and discharge process increases the charge consumption, as our model shows. The models in [23] and [24] plotted in Fig. 10(b) account only for the bottom parasitic capacitances, as it can be seen in (40). Nevertheless, the top parasitic capacitances also increase the charge consumed, as correctly predicted by our model.

The previous analysis has been extended to the FQP8 $\times$  and EQP8 $\times$  topologies. As these two converters feature a similar behavior and for the sake of brevity, the results are only shown for EQP8 $\times$  in Fig. 11(a)–(b). As we can see, the gain and time response are greatly affected by both parasitic capacitances. This causes a voltage drop from  $V_{out} = 2\ \text{V}$  for the ideal EQP8 $\times$  down to  $V_{out} = 0.87\ \text{V}$  as Fig. 11(a) shows. A similar conclusion is drawn when studying the charge consumed by FQP and EQP: including parasitic capacitances increases the charge consumed by the charge pump. Fig. 11(b) shows the situation for EQP8 $\times$ . Also, as in the previous analysis and as expected in the SSL mode, the model simulations match accurately experimental results and circuit-level simulations. The small differences between the model and the experimental results are mainly due to the capacitors tolerance.

Next, we study the accuracy of our model with charge reusing. The three main topologies are studied, showing an increase of the efficiency in all cases, but for the sake of brevity only the results for EQP8 $\times$  are shown in Fig. 12.

The charge reusing approach improves the gain of FQP and EQP. In EQP8 $\times$  with purely capacitive load, the gain increases from  $3.46\times$  for the standard charge pump solution to  $4.65\times$  for the charge pump with the charge reusing approach. For the same charge pump with current load, the gain increases from  $2.58\times$  to  $3.51\times$ . For FQP8 $\times$  with purely capacitive load, the gain is improved from  $4.84\times$  to  $5.79\times$  and for the same architecture with current load, the gain increases from  $3.98\times$  to  $4.75\times$ . Regarding the LQP, the gain remains the same with charge reusing as for the standard LQP architecture.

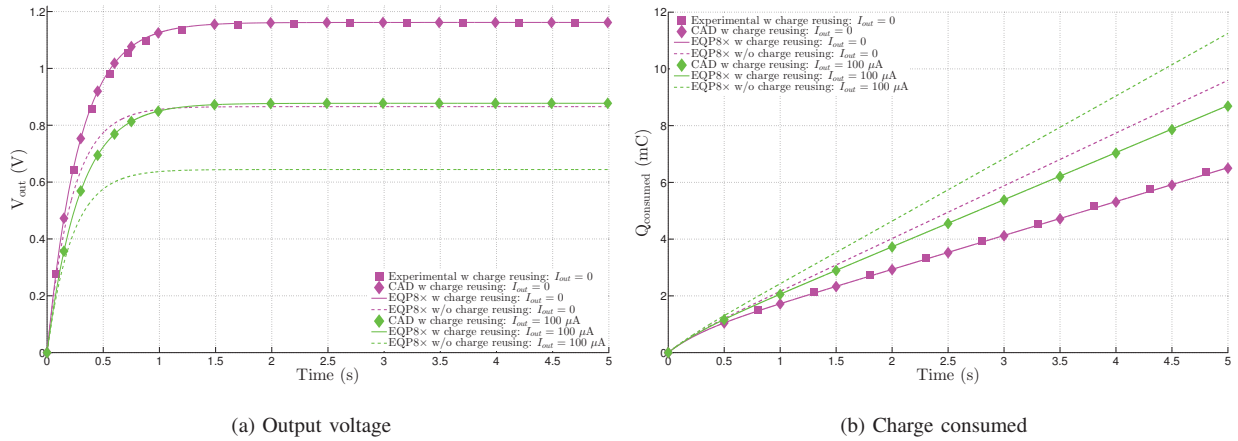

 Fig. 12. Comparison of the dynamic response for EQP8 $\times$  with and without charge reusing approach.

 TABLE V  
 COMPARISON OF THE THREE MAIN CAPACITIVE CHARGE PUMP TOPOLOGIES

	$\alpha$	$\beta$	$I_{out}(\mu A)$	LQP8 $\times$		FQP8 $\times$		EQP8 $\times$	
				Gain	$\Delta$ (%)	Gain	$\Delta$ (%)	Gain	$\Delta$ (%)
without charge reusing	0	0	0	8.00	0	8.00	0	8.00	0
without charge reusing	0.1	0.1	0	7.36	8.00	4.84	39.50	3.46	56.75
with charge reusing	0.1	0.1	0	7.36	8.00	5.79	27.62	4.65	41.88
without charge reusing	0	0	100	6.60	17.5	6.5	18.75	5.9	26.25
without charge reusing	0.1	0.1	100	6.09	23.88	3.98	50.25	2.58	67.75
with charge reusing	0.1	0.1	100	6.09	23.88	4.75	40.62	3.51	56.12

Table V summarizes the data addressed above for the different configurations and its deviation with respect to the ideal case,  $\Delta(\%)$ . As seen, the parasitic capacitances decrease the gain of all charge pumps, being EQP the most sensitive to them. For EQP8 $\times$  with  $\alpha, \beta = 0.1$  and without charge reusing, the deviation in the gain is 56.75%. The charge reusing approach improves the gain, decreasing this deviation to 41.88%. A current load also introduces a deviation in the gain. In EQP8 $\times$  with  $\alpha, \beta = 0.1$  and  $I_{out} = 100 \mu A$  without charge reusing the deviation is 67.75%, which decreases down to 56.12% with charge reusing.

With respect to the time response, the charge reusing technique does not modify the transient response of LQP, but it shortens the time response of FQP and EQP. Regarding the charge consumed, Fig. 12(b) shows how the charge consumed by the charge pump and, therefore, the efficiency is improved for EQP8 $\times$  when charge reusing is implemented.

Finally, we study the transient response of charge pumps driving both capacitor and dynamic loads. The dynamic load is implemented as a resistor  $R_L$  which is connected and disconnected to/from the charge pump in steady state through pulses triggered by the DAQ system. The effect of  $R_L$  is included in our model through the  $I_{out}$  term,

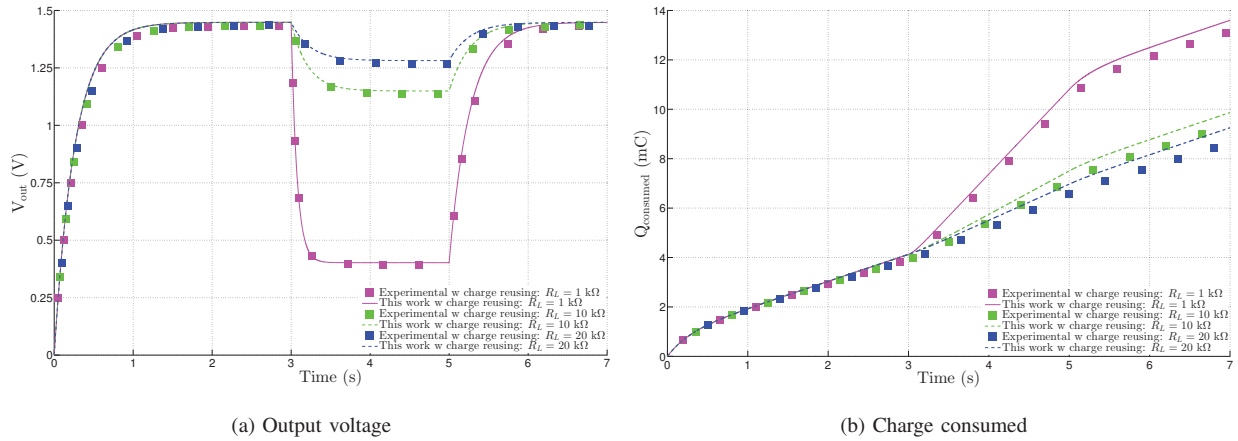


Fig. 13. Dynamic load response of an FQP8x with charge reusing.

which is assumed to be constant during each cycle and its value is updated through (41) and (42) in the rising edges of  $clk1$  and  $clk2$ , respectively.  $I_{out1}$  and  $I_{out2}$  replace  $I_{out}$  in  $\mathbf{K}_1$  and  $\mathbf{K}_2$  in (12) and (16).  $V_{i1}(C_s)$  and  $V_{i2}(C_s)$  represent the voltage at the storage capacitor,  $C_s$ , at the rising edge of  $clk1$  and  $clk2$ , respectively.

$$I_{out1} = \frac{V_{i1}(C_s)}{R_L} \quad (41)$$

$$I_{out2} = \frac{V_{i2}(C_s)}{R_L} \quad (42)$$

Fig. 13 compares both experimental results and simulations with our model for an FQP8x with parasitic capacitances and charge reusing for several values of  $R_L$ . During the steady state of the charge pump, at  $t = 3$  s, a switch connects  $R_L$  to the DC-DC converter for two seconds. The  $R_L$  is subsequently disconnected from the DC-DC converter at  $t = 5$  s. Fig. 13(a) shows the transient for the output voltage. We can see how  $V_{out}$  drops when  $R_L$  is connected. The smaller the resistor, the larger the voltage drop. Similarly, the smaller the resistor, the shorter the fall time, which is 0.16 s for  $R_L = 1$  kΩ and 0.51 s for  $R_L = 20$  kΩ. Fig. 13(a) also shows how the charge pump goes back to the previous steady state when the resistor load  $R_L$  is disconnected. Rise time is 0.58 s regardless of  $R_L$ , as rise times do not depend on the initial voltage at  $R_L$ . As Fig. 13(b) shows, smaller  $R_L$  values imply a larger amount of charge drained by the charge pump. The small differences between our model and the experimental results are mainly due to the capacitors tolerance.

We have also used our model to measure the output impedance,  $R_{out}$ , of a charge pump assuming a DC-DC converter model driving a storage capacitor  $C_s$  and a dynamic resistive load as that of Fig. 14. Signal  $\phi$  is provided by the DAQ board to set the dynamic load.  $R_{out}$  can be calculated through (43), where  $\Delta V$  is the voltage drop when  $R_L$  is connected and  $I_{R_L}$  the current through  $R_L$  in the steady state. The experimental procedure to measure  $R_{out}$  was to average the results from the three different load resistors of Fig. 13, i.e.,  $R_L = 1, 10$  and  $20$  kΩ. Deviations among  $R_{out}$  from such three  $R_L$  values are negligible. The measurements are in the range 2-25 kHz, guaranteeing that the DC-DC converter works within the SSL regime.

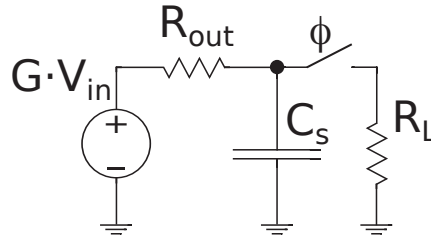


Fig. 14. Output impedance model of a capacitive DC-DC converter with dynamic load.

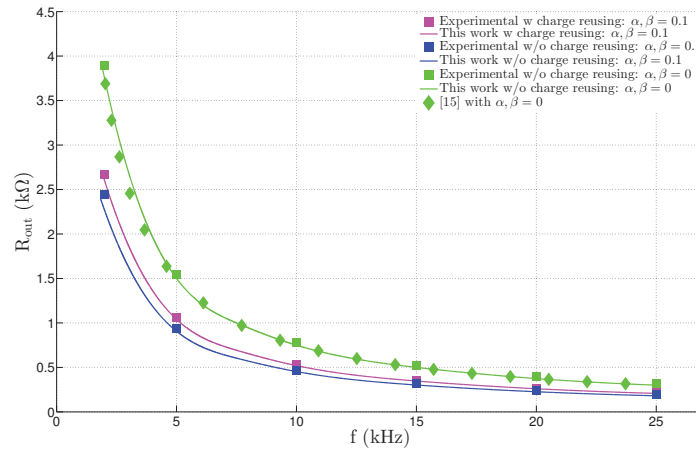


Fig. 15. Dependence of the output impedance with the switching frequency of FQP8x.

$$R_{out} = \frac{\Delta V}{I_{R_L}} \quad (43)$$

Fig. 15 shows experimental results along with theoretical values from both our model with and without charge reusing and parasitic capacitances and the model from [15] without charge reusing and without parasitic capacitances. Experimental results are in good agreement with theoretical expressions. We can also see that the lack of parasitic capacitances,  $\alpha, \beta = 0$ , leads to higher  $R_{out}$  values. Also, the charge reusing technique increases  $R_{out}$  slightly with respect to the case with  $\alpha, \beta \neq 0$  [13].

## V. DESIGN PROCEDURE

This section shows the design procedure of a charge pump with our model. The first subsection describes the guidelines for an easy use of our model in the design process of a DC-DC converter. In the last subsection, the design procedure is illustrated with a case study for energy harvesting.

### A. Guidelines To Use Our Model

Fig. 16 shows two flow diagrams which drive the design procedure for two different situations. The design with our web simulator follows such flow diagrams [34].

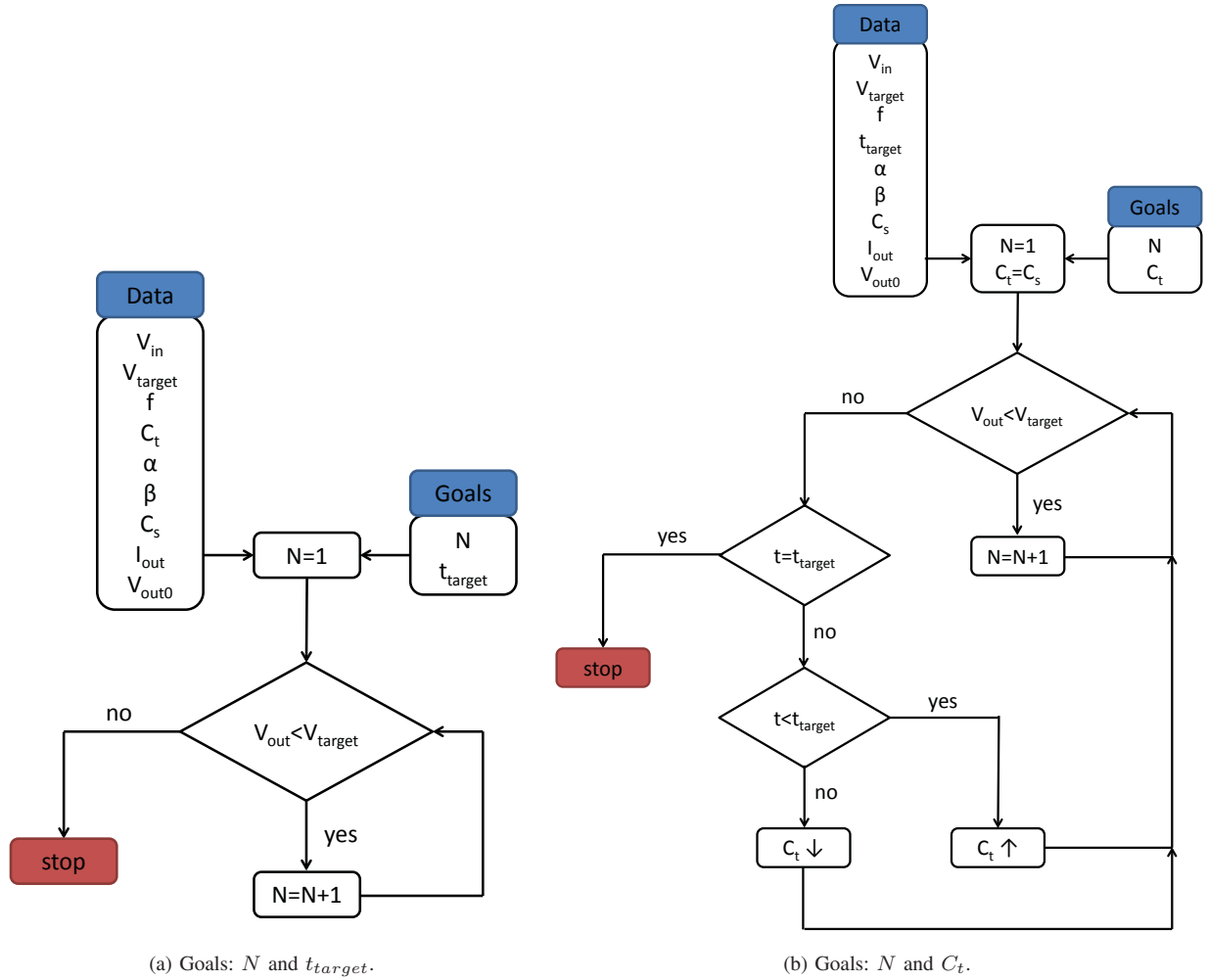


Fig. 16. Guidelines to design DC-DC converters with our model.

On the one hand, Fig. 16(a) describes a situation where the goals are the number of stages,  $N$ , and the time  $t_{target}$  needed to reach the target voltage,  $V_{target}$ . The input data depend on both the particular application ( $V_{in}$ ,  $f$ ,  $C_t$ ,  $C_s$ ,  $I_{out}$  and the voltage in  $C_s$  at  $t = 0$ ,  $V_{out0}$ ) and the technology ( $\alpha$  and  $\beta$ ). The iterative process starts with  $N = 1$  and then  $N$  is increased until  $V_{target}$  is reached. After that, more simulations with higher  $N$  can be run in order to find the optimal  $t_{target}$ .

On the other hand, Fig. 16(b) addresses the case where the goals are  $N$  and  $C_t$ , and  $t_{target}$  is fixed by the particular application. The iterative process starts with  $N = 1$  and  $C_t = C_s$ . When the minimum number of stages is found,  $C_t$  is modified to meet its optimum value.

### B. Case Study: Energy Harvesting

This subsection shows a case study of a charge pump circuit design based on the procedure of Fig. 16(a) for micro-energy harvesting. As an example of a practical case, in [35] or [36] a system with light energy harvesting

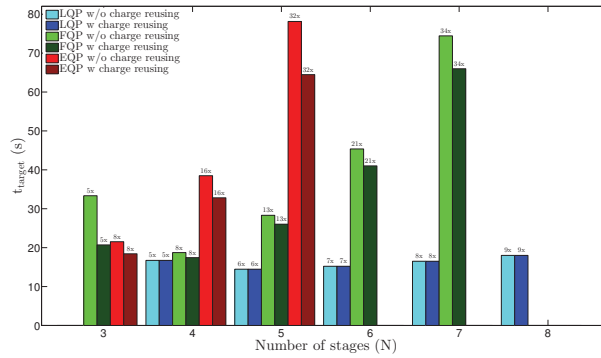


Fig. 17. Time needed to reach  $V_{out} = 1.8$  V from  $V_{in} = 0.4$  V for LQP, FQP and EQP with different gains.

capability is designed in which our model with our web simulator could be applied to design the DC-DC converter.

For a given area, there are two main performance metrics of interest in the design of charge pumps for micro-energy harvesting, namely, 1) charge efficiency measured through the charge drawn by the charge pump from the energy transducer, which should be as low as possible, and 2) the time it takes the charge pump to rise up the voltage produced by the energy transducer to the voltage of interest,  $t_{target}$ , which should be as short as possible too. As it will be shown below, charge efficiency and time response make up a trade-off in the design space. The simulations shown in this section are intended for a micro photovoltaic cell in standard  $0.18 \mu\text{m}$  CMOS technology with  $V_{DD} = 1.8$  V. The design procedure is illustrated with and without the charge reusing approach.

Concerning the parameters for our simulator, we have assumed a given area of  $0.1 \text{ mm}^2$  for the charge pumps, which for a standard MIM technology ( $1 \text{ fF}/\mu\text{m}^2$ ) means a total capacitance of  $C_t = 100 \text{ pF}$ . The clock cycle for  $clk1$  and  $clk2$  is set as  $T = 4 \mu\text{s}$  with transmission gates at minimum size, and  $clk3$  is set as  $T = 2 \mu\text{s}$  with a pulse width of  $40 \text{ ns}$ . These parameters make (33) comply with the operating condition in the SSL regime. In energy harvesting applications the charge pump load is purely capacitive to store the energy harvested, so  $I_{out} = 0$ , while  $C_s = 10 \mu\text{F}$  is chosen as storage capacitor. It should be noted that  $C_j \ll C_s$ , which occurs when the energy transducer and the circuit to which the energy scavenged from the environment is supplied share the same silicon substrate [41].  $V_{in} = 0.4$  V is taken as a typical voltage that can be produced by a micro photovoltaic DC energy transducer.

Fig. 17 shows the time needed to reach  $V_{DD}$  by LQP, FQP and EQP under the constraint of the same area. Different number of stages are compared, and the minimum gain shown is the minimum gain to reach  $V_{DD}$ . In the case of LQP,  $6\times$  gain provides the fastest response. For FQP and EQP,  $8\times$  gain is the best solution in both cases, without and with charge reusing. Concerning charge consumed or similarly for charge efficiency, a topology with less stages consumes less charge as Fig. 18 shows. A  $5\times$  gain is the best option for LQP and FQP, and  $8\times$  gain for EQP. Comparing all data for the three topologies, LQP provides the fastest response, and also, it is the solution with the best charge conversion efficiency ( $6\times$  and  $5\times$  gains respectively).

Analyzing Fig. 17 and Fig. 18, we see that, in general, the solution that minimizes the time response is not the

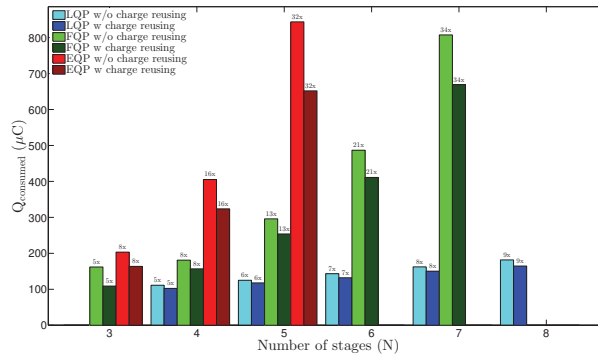


Fig. 18. Charge needed to reach  $V_{out} = 1.8$  V from  $V_{in} = 0.4$  V for LQP, FQP and EQP with different gains.

same that minimizes charge consumption. Nevertheless, particular design conditions might lead to solutions that optimize both charge conversion efficiency and time response. This is the case of EQP8×.

## VI. CONCLUSION

This paper introduces an accurate model of the dynamic behavior of standard two-phase switched-capacitor DC-DC converters and their charge reusing version with top and bottom parasitic capacitances in the SSL regime. The model was illustrated for three well-known capacitive DC-DC converter topologies, i.e., LQP, FQP and EQP. The charge reusing approach reduces the charge consumed by LQP and both gain and charge consumed for FQP and EQP. The paper addresses a methodology to design the DC-DC converter outside the SSL regime with a given error level with respect to circuit-level simulations in the switching frequency and switching transistor width parameter space. It includes a validation with experimental results and circuit-level simulations in the SSL region, as well as a comparison with other models in the literature for LQP, FQP and EQP for both current and capacitive loads. The model also tackles dynamic loads, that combined with transient analysis permit to measure the output impedance of the DC-DC converter under study. Our model accounts for actual conditions that are not included in other models in the literature, featuring more accurate results. From the developed model, a web simulator that is up to 10000× faster than circuit-level simulators is built. As an example of applicability, the model in this paper is used as a design tool to choose the best configuration in terms of speed and charge conversion efficiency for micro-energy harvesting constraints.

APPENDIX A  
MATRICES

Matrices  $\mathbf{V}_{i1}$ ,  $\mathbf{V}_{e1}$ ,  $\mathbf{Q}_1$ ,  $\mathbf{V}_{i2}$ ,  $\mathbf{V}_{e2}$ ,  $\mathbf{Q}_2$ ,  $\mathbf{C}$ ,  $\mathbf{P}$ ,  $\mathbf{W}_1$ ,  $\mathbf{W}_2$ ,  $\mathbf{M}$ ,  $\mathbf{N}_1$  and  $\mathbf{N}_2$  defined in Section III were obtained following the procedure in [27]. In order to make this paper self-contained we list such matrices below.

$$\mathbf{V}_{i1} = \begin{pmatrix} V_{in} \\ V_{i1}(\alpha C_j) \\ V_{i1}(C_j) \\ V_{i1}(\beta C_j) \\ \vdots \\ V_{i1}(\alpha C_N) \\ V_{i1}(C_N) \\ V_{i1}(\beta C_N) \\ V_{i1}(C_s) \end{pmatrix} \quad (44) \quad \mathbf{v}_{e1} = \begin{pmatrix} V_{in} \\ V_{e1}(\alpha C_j) \\ V_{e1}(C_j) \\ V_{e1}(\beta C_j) \\ \vdots \\ V_{e1}(\alpha C_N) \\ V_{e1}(C_N) \\ V_{e1}(\beta C_N) \\ V_{e1}(C_s) \end{pmatrix} \quad (45)$$

$$\mathbf{Q}_1 = \begin{pmatrix} Q_1(V_{in}) \\ Q_1(\alpha C_j) \\ Q_1(C_j) \\ Q_1(\beta C_j) \\ \vdots \\ Q_1(\alpha C_N) \\ Q_1(C_N) \\ Q_1(\beta C_N) \\ Q_1(C_s) \end{pmatrix} \quad (46) \quad \mathbf{v}_{i2} = \begin{pmatrix} V_{in} \\ V_{i2}(\alpha C_j) \\ V_{i2}(C_j) \\ V_{i2}(\beta C_j) \\ \vdots \\ V_{i2}(\alpha C_N) \\ V_{i2}(C_N) \\ V_{i2}(\beta C_N) \\ V_{i2}(C_s) \end{pmatrix} \quad (47)$$

$$\mathbf{V}_{e2} = \begin{pmatrix} V_{in} \\ V_{e2}(\alpha C_j) \\ V_{e2}(C_j) \\ V_{e2}(\beta C_j) \\ \vdots \\ V_{e2}(\alpha C_N) \\ V_{e2}(C_N) \\ V_{e2}(\beta C_N) \\ V_{e2}(C_s) \end{pmatrix} \quad (48) \quad \mathbf{Q}_2 = \begin{pmatrix} Q_2(V_{in}) \\ Q_2(\alpha C_j) \\ Q_2(C_j) \\ Q_2(\beta C_j) \\ \vdots \\ Q_2(\alpha C_N) \\ Q_2(C_N) \\ Q_2(\beta C_N) \\ Q_2(C_s) \end{pmatrix} \quad (49)$$

$$\mathbf{C} = \text{diag}\{0, \frac{1}{\alpha C_j}, \frac{1}{C_j}, \frac{1}{\beta C_j}, \dots, \frac{1}{\alpha C_N}, \frac{1}{C_N}, \frac{1}{\beta C_N}, \frac{1}{C_s}\} \quad (50)$$

$$\mathbf{P} = (\mathbf{I} - \mathbf{C}\mathbf{A}_2^{-1}\mathbf{B}_2)(\mathbf{I} - \mathbf{C}\mathbf{A}_1^{-1}\mathbf{B}_1) \quad (51)$$

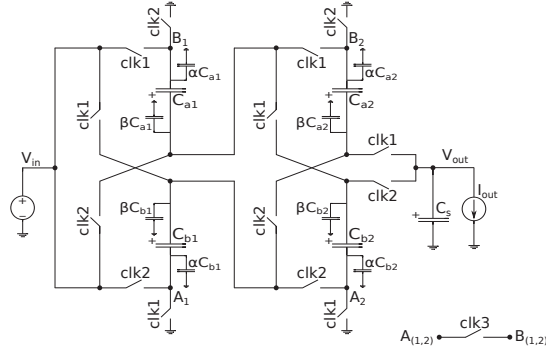


Fig. 19. Schematic of an exponential charge pump with  $4\times$  gain. The additional switch for charge reusing is driven by  $clk3$ .

$$\mathbf{W}_1 = (\mathbf{I} - \mathbf{C}\mathbf{A}_2^{-1}\mathbf{B}_2)\mathbf{C}\mathbf{A}_1^{-1} \quad (52)$$

$$\mathbf{W}_2 = \mathbf{C}\mathbf{A}_2^{-1} \quad (53)$$

$$\mathbf{M} = \mathbf{A}_2^{-1}\mathbf{B}_2(\mathbf{C}\mathbf{A}_1^{-1}\mathbf{B}_1 - \mathbf{I}) - \mathbf{A}_1^{-1}\mathbf{B}_1 \quad (54)$$

$$\mathbf{N}_1 = (\mathbf{I} - \mathbf{A}_2^{-1}\mathbf{B}_2\mathbf{C})\mathbf{A}_1^{-1} \quad (55)$$

$$\mathbf{N}_2 = \mathbf{A}_2^{-1} \quad (56)$$

## APPENDIX B

### MODEL EXTENSION TO THE FQP AND EQP TOPOLOGIES

The model for any capacitive charge pump circuit including both top and bottom parasitic capacitances was illustrated with LQP $3\times$  in Section III. In this Appendix and without loss of generality, the model is illustrated for FQP $3\times$  and EQP $4\times$ .

Fig. 19 represents the schematic of an exponential charge pump with gain  $4\times$ . In this case, since EQP $4\times$  has two branches with two capacitors each, the matrices resulting from applying KVL and KCL to this topology have a dimension of  $14\times 14$ . They are shown in (57)–(62).

Fig. 20 represents the schematic of a double Fibonacci charge pump with gain  $3\times$ . This configuration is implemented as a parallel connection of two standard FQP in opposite phases. In the SSL regime, the behavior of a double FQP is similar to the standard FQP when the total capacitance,  $C_t$ , is the same. This structure is needed to implement the charge reusing technique. The matrices required to apply our model in this case are (63)–(68).





$$\mathbf{A}_2 = \begin{pmatrix} 0 & \frac{-1}{\alpha C_{a1}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{\alpha C_{a1}} & \frac{1}{C_{a1}} & \frac{-1}{\beta C_{a1}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{\alpha C_{a2}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{\beta C_{a1}} & 0 & \frac{-1}{C_{a2}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_{a2}} & \frac{-1}{\beta C_{a2}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{\alpha C_{b1}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_{b1}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_{b1}} & \frac{-1}{\beta C_{b1}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{\beta C_{b1}} & \frac{-1}{\alpha C_{b2}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{\alpha C_{b2}} & \frac{1}{C_{b2}} & \frac{-1}{\beta C_{b2}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{\beta C_{b2}} & \frac{-1}{C_s} & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 & -1 & -1 & -1 & 1 & 0 & 0 \\ 0 & 0 & -1 & -1 & 0 & -1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & -1 & -1 \end{pmatrix} \quad (66)$$

$$\mathbf{B}_2 = \begin{pmatrix} 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix} \quad (67)$$

$$\mathbf{K}_2 = \left( 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ I_{out} T(1-D) \right)^t \quad (68)$$

#### ACKNOWLEDGMENT

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