Random Dopant, Line-Edge Roughness and Gate Workfunction Variability in a Nano InGaAs FinFET

N. Seoane, G. Indalecio, E. Comesaña, M. Aldegunde, A. J. García-Loureiro and K. Kalna

***Abstract*—A 3D quantum-corrected drift-diffusion simulation study of three sources of statistical variability including discrete random dopants (RD), line-edge roughness (LER) and metal gate workfunction (MGW) was performed for a 14 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET in the subthreshold region using Fermi-Dirac statistics. The study has been done at both low (0.05 V) and high drain biases (0.6 V). The LER variability is characterised by the root mean square amplitude (Δ) and correlation length (Λ), and the MGW variability by the metal grain size (GS). The RD induced variation $\sigma V_T = 6$ mV is similar to that observed in Si SOI FinFETs. The LER induced threshold voltage variations ($\sigma V_T < 6$ mV) are similar to RD variations when Δ=1 nm, and smaller than the observed in Si SOI FinFETs (around 18 mV). For larger Δ, the LER exhibits σV_T ranging from 11 mV when Λ=10 nm and Δ=2 nm to 19 mV when Λ=20 nm and Δ=3 nm. The MGW variations are the dominant source of variability in the subthreshold characteristics, the σV_T ranges from 106 mV when GS=10 nm to 43 mV when GS=3 nm which is larger than those observed in equivalent TiN metal-gate Si FinFETs.**

***Index Terms*—Intrinsic parameter fluctuations, random dopant, line-edge roughness, gate workfunction variability, III-V materials, FinFETs.**

I. Introduction

TRANSISTORS with channels based on III-V compounds are intensively researched [1], [2] due to their high injection velocity and electron mobility [3], [4] which can be more than 10 times larger than in Si devices for the same sheet density. The III-V channels combined with a multigate structure mitigate the negative effects of the low density of states of III-V semiconductors making them promising candidates for the 14 nm technology node and beyond [5].

However, a major issue affecting scaling and integration of any nano-transistor is the device variability that affects its characteristics. Even though a multigate structure ensures a much better control of the carriers in the channel, variability effects in the subthreshold region might limit their integration into CMOS technology [6]. Among them, random dopant (RD) fluctuations, line-edge roughness (LER) and metal-gate workfunction (MGW) variations have the strongest effect on the performance and reliability of both Si and III-V channel based nano-MOSFETs fabricated using planar [7], [8] or non-planar architectures [9], [10]. III-V non-planar transistors may be potentially more resilient to variability than the corresponding Si devices as reported recently for the 22-nm technology node [11].

This work is supported by Marie-Curie Fellowship (PIEF-GA-2011-299990), EPSRC (EP/I010084/1), Spanish Government (TEC2010-17320) and Xunta de Galicia (2010/28). Authors thank CESGA for the access granted to the SVGD.

G. Indalecio, E. Comesaña, and A. J. García-Loureiro are with the CITIUS, University of Santiago de Compostela, Galicia, Spain.

N. Seoane, M. Aldegunde and K. Kalna are with the Electronic Systems Design Centre, College of Engineering, Swansea University, Wales, United Kingdom. e-mail: (N.S.Iglesias@swansea.ac.uk)

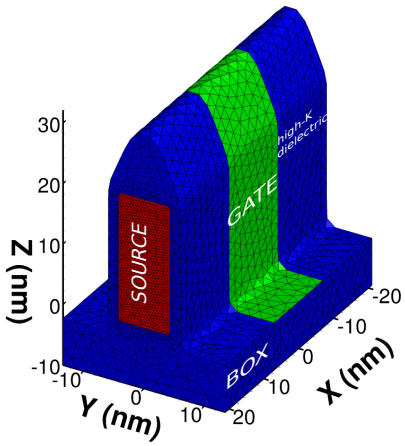


Fig. 1. Schematic view of the 14 nm gate length III-V FinFET showing the tetrahedral mesh.

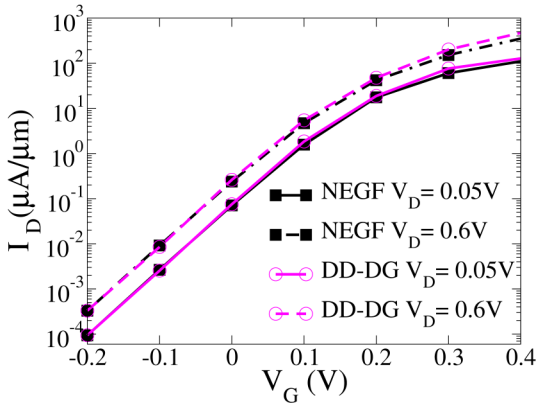


Fig. 2. I_D-V_G characteristics comparing results from the 3D quantum corrected DD simulations (DD-DG) to NEGF Silvaco simulations.

In this work, we study the RD, LER and MGW fluctuations affecting the subthreshold region of a 14 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET. We simulate the variability in device threshold voltage (V_T), off-current (I_{OFF}), subthreshold slope (SS) and drain-induced-barrier-lowering (DIBL) at both low and high drain biases. The simulations have been performed using our established 3D drift-diffusion (DD) simulation approach for III-V materials [7], [9] that uses Fermi-Dirac statistics and incorporates the quantum mechanical confinement effects using a finite-element (FE) implementation of the density gradient (DG) model [12].

II. Device structure and calibration process

Fig. 1 depicts the structure of the simulated III-V FinFET. The device has a gate length of 14 nm, an $In_{0.53}Ga_{0.47}As$ channel, *p*-type doped to $10^{17}cm^{-3}$, 14 nm *n*-doped source/drain (S/D) regions, a fin width of 8.5 nm and a fin height of 21.25 nm (assuming a ratio $\sim 1:2.5$). The body of semiconductor is surrounded by a high-κ dielectric with an equivalent oxide thickness (EOT) of 0.68 nm and by a 10 nm buried oxide (BOX). All the device dimensions follow the scaling predictions for III-V FinFETs given by ITRS 2011 [13]. The S/D doping was generated using an analytical profile with a peak value of $5x10^{19}cm^{-3}$ and a Gaussian decay of δ=2.5 nm. Fig. 1 also shows the tetrahedral mesh used in all the simulations except for the MGW variability, that required a more refined mesh in the metal gate region.

In this study, we use our in-house parallel 3D FE DD device simulator [7] that incorporates the quantum confinement effects via an optimised FE density gradient approach for multi-gate transistors [14]. Considering the level of degeneracy in the S/D regions of the semiconductor, we have to consider Fermi-Dirac statistics in our simulations [15]. We calibrate the DD simulator in the subthreshold region by matching its I_D-V_G characteristics against Silvaco's 3D ballistic non-equilibrium Green's function (NEGF) simulations [16] at both low and high drain biases, as can be seen in Fig. 2, with a very good agreement in the subthreshold region.

The electron effective masses in the $In_{0.53}Ga_{0.47}As$ region and in the oxide used in the DG approach act just as calibration parameters [9], [17], representing the strength of the confinement. An increase (decrease) in these masses along the *y* and *z*-directions will reduce (increase) the transversal confinement of the electrons in the channel producing a threshold voltage shift. The mass in the *x*-direction partially accounts for the source-to-drain tunnelling in the subthreshold region. An increase (decrease) in this mass will be reflected in an improvement (worsening) in the subthreshold slope of an I_D-V_G characteristic. Note that since these electron effective masses are just fitting parameters they have no relation with the transport effective masses in InGaAs. At a low drain bias of 0.05 V, the electron effective masses were set to $0.30m_0$ in *x*, *y* and *z*-directions. At a high drain bias of 0.6 V, the electron effective masses were determined to be $0.14m_0$ in *x*-direction, and $0.01m_0$ in *y* and *z*-directions. The effective mass for the oxide was set to $0.2m_0$ for both low and high V_D.

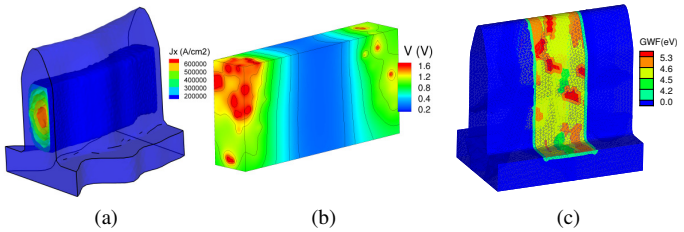
The 14 nm $In_{0.53}Ga_{0.47}As$ FinFET device shows excellent off-state characteristics with a subthreshold slope (SS) of 70 mV/dec and a drain-induced barrier lowering (DIBL) of 37 mV/V. The threshold voltages of the device obtained from linear extrapolation at drain biases of 0.05 and 0.6 V are V_{Tlow}=0.18 V and V_{Thigh}=0.2 V, respectively. The work function of the metal was set to 4.7 eV.

III. Simulation methodology

We have obtained the LER profiles from the Fourier synthesis method, as described in [8], parameterised by the correlation length (Λ=10 and 20 nm) and the root mean square (Δ=1, 2 and 3 nm) [11], [18], [19]. The method is based on the inverse discrete transformation, and consists on the application of a Gaussian filter over a list of random phases. The width of the Gaussian filter will account for the correlation length, and the amplitude will set the root mean square value. To model the Fourier spectra, we use the following autocorrelation function:

$$S_G(k) = \sqrt{\pi}\Delta^2\Lambda e^{(-k^2\Lambda^2/4)} \quad (1)$$

In this study, we simulate the influence of uncorrelated fin edge roughness. Fig. 3(a) represents the current density along the transport direction for a particular LER profile with Λ=20 nm and Δ=2 nm at the threshold voltage gate bias.



(a) (b) (c)

Fig. 3. (a) Iso-surfaces showing the current density along the *x*-direction inside the $In_{0.53}Ga_{0.47}As$ device body for a particular LER profile at V_G=V_T and V_D=0.05 V, (b) Electrostatic potential inside the $In_{0.53}Ga_{0.47}As$ region for a pattern of RDs at V_G=V_T and V_D=0.05 V and (c) Example of the metal gate workfunction variation for a 3 nm grain size.

To model the RD variability, we have obtained different device configurations with different positions of dopants in the $In_{0.53}Ga_{0.47}As$ region by implementing a rejection technique from the device with the analytical doping profile (continuous device). Fig. 3(b) shows an example of the potential distribution generated by a particular configuration of random dopants inside the semiconductor at V_D=0.05 V and V_G=V_T.

To model the dependence of the metal gate workfunction on the granularity [20], [21], [22], we follow the methodology described in [23]. We calculate a Voronoi diagram of a set of randomly generated points, which varies the size and shape of the grains. We assign a certain orientation to each polygon based on the experimental probability of occurrence. This approach provides a more realistic physical representation of the grains than the usual square grain approximation [23]. The device has a WN metal gate. For this particular metal gate we have to define four possible orientations of the grains with MGWs of 4.5, 4.6, 5.3 and 4.2 eV, and probabilities of occurrence 65%, 15%, 15% and 5%, respectively [24]. We study four average grain diameters (10, 7, 5 and 3 nm). Fig. 3(c) shows the effect of a Voronoi profile, for a 3 nm average grain diameter, in the gate workfunction potential of the device.

We have simulated ensembles of 300 device configurations for each source of variability and for each fluctuation parameter, extracting their average values (mean) and standard deviations (σ). To estimate the threshold voltage, we have used a constant current criterion ($I_T = 7.5 \times 10^{-7}$ A and 3.0×10^{-6} A at V_D=0.05 V and 0.6 V, respectively). To extract the DIBL, we have consider the barrier lowering at the point where V_G=V_T and V_D=0.05 V.

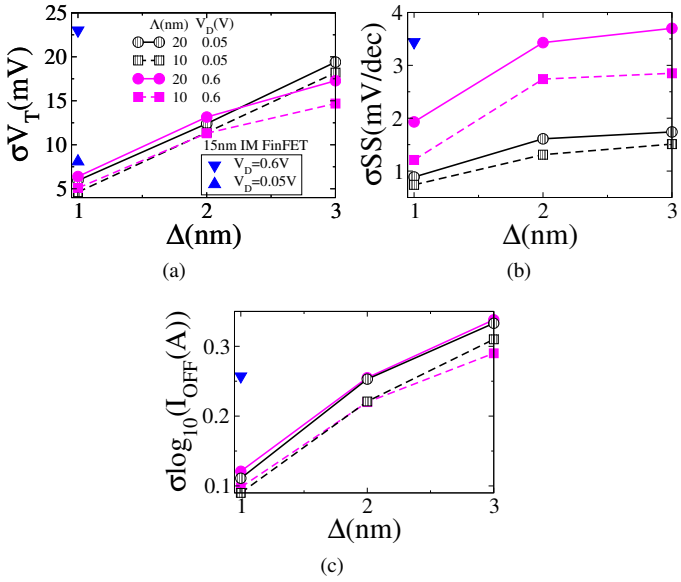


Fig. 4. V_T, SS and I_{OFF} standard deviations due to LER fluctuations as a function of Λ, Δ and the drain bias. The corresponding variability data for a 13 nm gate length Si inversion-mode FinFET (when Λ=15 nm) [19] has been included for comparison (blue triangles).

A. Line edge roughness variability

Fig. 4 shows the threshold voltage, subthreshold slope, and off-current standard deviations due to the LER variability as a function of Λ, Δ and the applied drain bias. As expected, the standard deviations in the three figures of merit increase when Λ or Δ are increased. At low drain bias, the observed V_T standard deviation is approximately linearly proportional to the root mean square amplitude of the LER and can reach up to 19.4 mV for Λ=20 nm and Δ=3 nm. At V_D=0.6 V, for Δ values lower than 3 nm, the threshold voltage variability is slightly larger than at low drain bias and follows the same trend. However, when Δ=3 nm, the V_T standard deviation is lower at high drain than at low drain bias. The increase in the drain bias also leads to an increase in the SS variability, with the SS standard deviations twice as large, reaching up to 3.7 mV/dec for Λ=20 nm and Δ=3 nm.

Table I shows the LER induced V_T, SS, I_{OFF} and DIBL shifts for the different Λ and Δ values at high drain bias. In order to clarify the terminology used, we define, for a given variable X, the X_{shift} as the difference between the mean value of the statistical sample, $\langle X \rangle$, and the value of the magnitude for the continuous device, X_0. There is a linear increase in V_{Tshift} with Δ which is slightly larger for Λ=10 nm. V_{Tshift} is always positive and ranges from 11 mV when Λ=20 nm and Δ=1 nm to 41 mV when Λ=10 nm and Δ=3 nm. The shift in the SS is very small, with up to an 6% change when Λ=20 nm and Δ=1 nm. The $DIBL_{shift}$ increases with an increase in the correlation length and with a reduction in the Δ value, reaching up to 15 mV/V.

The LER induced V_T variations (for Δ=1 nm and Λ=20 nm) are smaller at both low and high drain biases than the ones observed in a 13 nm gate length Si inversion-mode (IM) FinFET (for the same Δ and Λ=15 nm) [19]. The standard

TABLE I

LER INDUCED V_T, SS AND I_{OFF} SHIFTS AT A DRAIN BIAS OF 0.6 V AND THE CORRESPONDING SHIFT IN THE DIBL. FOR THE FOUR FIGURES OF MERIT, THESE SHIFTS REPRESENT THE DIFFERENCE BETWEEN THE MEAN VALUE OF THE STATISTICAL SAMPLE AND THE VALUE OF THE MAGNITUDE FOR THE CONTINUOUS DEVICE.

Λ (nm)	Δ (nm)	V_{Tshift} (mV)	SS_{shift} (mV/dec)	$\log_{10}(I_{OFF})_{shift}$ (A)	$DIBL_{shift}$ (mV/V)
10	1	12	3.7	0.025	14
	2	27	-2.3	-0.26	9.1
	3	41	-2.8	-0.52	7.3
20	1	11	4.2	0.049	15
	2	24	1.0	-0.19	11
	3	36	-1.3	-0.41	8.9

deviations for V_T are very affected by the drain bias in the Si IM FinFET (σV_T rises from 8.1 mV at V_D=0.05V to 22.9 mV at V_D=0.73V). However, for the InGaAs FinFET, the augmentation in σV_T with V_D is very small (σV_T rises from 5.9 mV at V_D=0.05V to 6.4 mV at V_D=0.6V). Comparing the other figures of merit for both device technologies at high drain bias, we observe that the standard deviations are also lower for the SS (σSS of 1.93 mV/dec for the InGaAs FinFET versus 3.44 mV/dec for the Si IM FinFET), the off-current (σI_{OFF}=18.4 nA/μm for the InGaAs FinFET versus 29.2 nA/μm for the IM Si FinFET) and the DIBL (σDIBL of 3.06 mV/V for the InGaAs FinFET versus 15.5 mV/V for the Si IM FinFET). These results show that the electron density is much better confined in the channel of the 14 nm gate length InGaAs FinFET than in the equivalent gate length Si devices making the device more resilient to the variability.

Figs. 5(a) and (b) represent the normal Q-Q plot of the V_T distribution due to LER for Λ=10 nm and Λ=20 nm, respectively, as a function of Δ and the theoretical quantiles from the normal distribution (black dashed lines). These results have been obtained at V_D=0.6 V. For Δ=1 nm, the data are close to a Gaussian distribution. When Δ increases we observe a shift in the curves, associated with an increase in the mean value of the distribution (see Table I for the exact figures of the threshold voltage shift). When Δ increases the data moves away from a Gaussian distribution in the tails, and the slope of the curves, which is proportionally related to the standard deviation of the distribution, increases. The change in the slope, and consequently the increase in σV_T, is more pronounced when Δ rises from 1 nm to 2 nm than from 2 nm to 3 nm [see Fig. 4(a)].

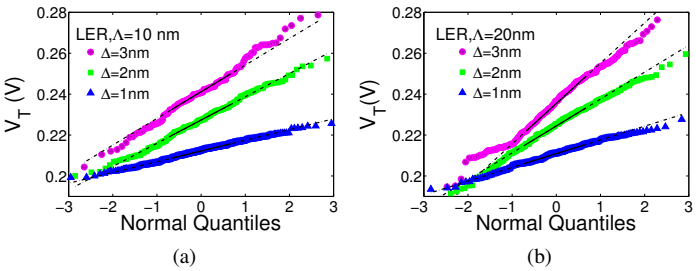


Fig. 5. Quantile-quantile plots of the V_T distribution due to LER variability for Λ=10 nm (a) and Λ=20 nm (b). The theoretical quantiles from the normal distribution are also represented (black dashed lines).

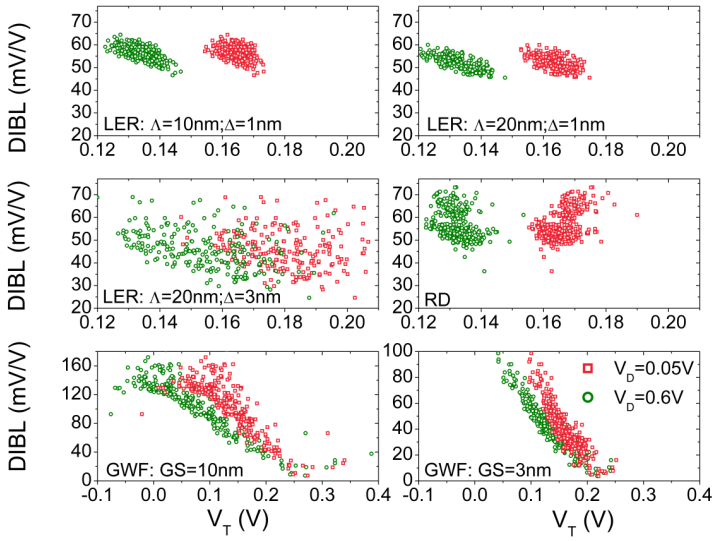


Fig. 6. Scatter plots showing the DIBL variation as a function of V_T, at both low and high drain biases, due to LER, RD and MGW fluctuations.

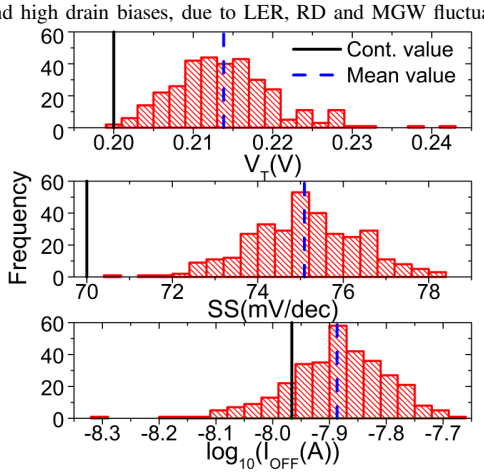


Fig. 7. Distribution of threshold voltages, subthreshold slopes and off–currents due to RD fluctuations in the $In_{0.53}Ga_{0.47}As$ region. The mean value of the statistical ensemble and the continuous device value are also indicated for comparison.

Fig. 6 shows the DIBL variation with V_T, at both low and high drain biases, due to LER (for three different Λ and Δ combinations), RD and MGW (for two different grain sizes) variability. When Δ=1 nm (see top two figures), the DIBL variation is very small (of around 3 mV/V for both Λ=10 nm and 20 nm) and it shows negative correlations with both V_{Tlow} and V_{Thigh}, exhibiting correlation coefficients (CC) of -0.5 and -0.7, respectively. When Δ=3 nm (middle figure in the left column), the variability in the DIBL triples and the correlation with the threshold voltages fades away (the CC are -0.1 and -0.4 with V_{Tlow} and V_{Thigh}).

B. Random dopant variability

Fig. 7 shows the V_T, SS and I_{OFF} variability due to the combined effect of *n*-type dopants present in the S/D regions and *p*-type dopants distributed along the channel. At V_D=0.6 V, the spreads in V_T, SS and $\log_{10}(I_{OFF})$ are 6.3 mV, 1.3 mV/dec and 0.089, respectively. The RD induced

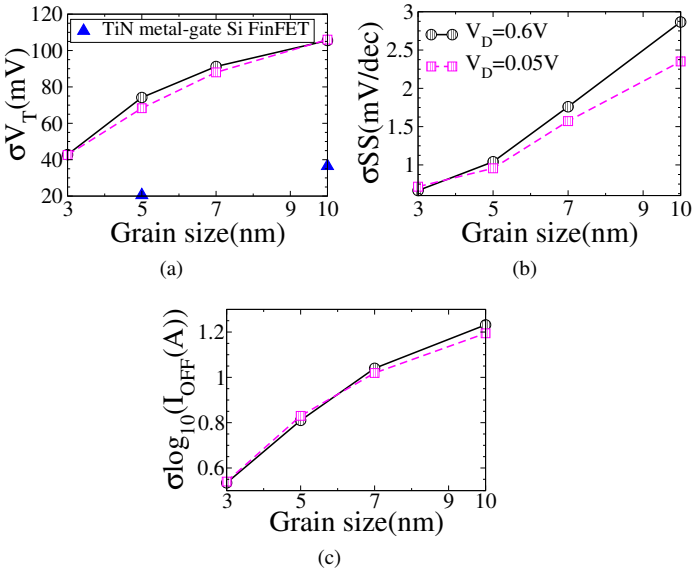


Fig. 8. V_T, SS and I_{OFF} standard deviations due to MGW fluctuations as a function of the grain size and the supply voltage. The σV_T for a TiN metal-gate FinFET with the equivalent gate length [10] is also shown for comparison (blue triangles). Note here that the difference in workfunctions between the two different grain orientations in the TiN metal-gate is 0.2 V, while for the WN metal-gate the largest difference in workfunction values is 1.0 V.

V_T, SS and $\log_{10}(I_{OFF})$ shifts are 14 mV, 5.1 mV/dec and 0.080. The distributions are close to a normal distribution and their standard deviations are very similar to those observed in the LER variability when Δ=1 nm. σV_T is dramatically reduced compared to planar bulk MOSFETs [6] thanks to the superior electrostatic integrity and tolerance to the low channel doping in the FinFET structure. The spread in V_T is similar to those observed in equivalent gate length FinFETs on SOI substrate [10]. On the other hand, the standard deviation of the DIBL is 6.4 mV/V, a value twice as large as the one observed in the LER variability when Δ=1 nm. Similarly, the RD induced DIBL shift (19.5 mV/V) is larger than in the LER variability independently of the Δ value. Fig. 6 shows the DIBL variation as a function of V_{Tlow} and V_{Thigh} due to RD (middle figure in the right column). The DIBL has weak correlations with the threshold voltage, which are positive for V_{Tlow} (CC=0.5) and negative for V_{Thigh} (CC=-0.3).

C. Metal gate workfunction variability

Fig. 8 shows the threshold voltage, subthreshold slope, and off-current standard deviations due to the MGW variability as a function of the grain size and the applied drain bias. As expected, the standard deviation of the three figures of merit increases with a growing metal grain diameter. At high drain bias, the increase in the grain size from 3 nm to 10 nm increases the spread in V_T, SS and $\log_{10}(I_{OFF})$ by 2.5, 4.3 and 2.3 times, respectively. The impact of the V_T fluctuations increases slightly with the applied drain bias up to a grain size of 10 nm, where σV_T at low and high drain biases is almost identical (σV_T=106 mV). This is due to the smaller effective gate affected for the variability when V_D=0.6 V [see Fig. 9(a)]. $\sigma\log_{10}(I_{OFF})$ is less affected by the drain bias

TABLE II
MGW INDUCED V_T, SS AND I_{OFF} SHIFTS AT A DRAIN BIAS OF 0.6 V AND THE CORRESPONDING SHIFT IN THE DIBL. FOR THE FOUR FIGURES OF MERIT, THESE SHIFTS REPRESENT THE DIFFERENCE BETWEEN THE MEAN VALUE OF THE STATISTICAL SAMPLE AND THE VALUE OF THE MAGNITUDE FOR THE CONTINUOS DEVICE.

Grain size (nm)	V_{Tshift} (mV)	SS_{shift} (mV/dec)	$\log_{10}(I_{OFF})_{shift}$ (A)	$DIBL_{shift}$ (mV/V)
10	31	0.40	0.64	67
7	8.5	0.73	0.46	28
5	42	1.0	0.099	11
3	40	1.5	-0.020	2.8

and it can reach up to 1.23. At high drain bias, we observe that the MGW variability (for the 10 nm grain size) induced threshold voltage and off-current standard deviations are 6 and 3 times larger, respectively, than the worst-case-scenario LER values (Λ=20 nm and Δ=3 nm). The SS variability also increases with the applied drain bias, observing SS standard deviations up to 2.9 mV/dec when GS=10nm. Note that we have obtained higher SS variability values due to LER variability when Λ=20 nm and $\Delta >$1 nm. An equivalent gate length TiN metal-gate Si FinFET with a 10 nm grain size has the σV_T significantly smaller (around 40 mV) [10] than that observed for the III-V FinFET (106 mV). TiN metal grains have 2 different possible grain orientations with MGW spanning 0.2 eV. The WN metal grains have a larger difference in their workfunctions (of around 1.0 eV), which explains a larger variability observed in the III-V FinFET.

Table II shows at V_D=0.6 V, the MGW induced V_T, SS, I_{OFF} and DIBL shifts for the different grain sizes. The maximum V_{Tshift} is 42 mV, a similar value that the one obtained for the LER variability when Λ=10 nm and Δ=3 nm. There is a increase in the SS shift with an reduction in the grain size, and the shift values are similar or even smaller than the ones observed in the LER variability. The $\log_{10}(I_{OFF})$ and DIBL shifts increase with an increase in the grain size, reaching up to 0.64 mV/V and 67 mV/V when GS=10 nm, respectively.

Figure 9(b) shows the normal Q-Q plot of the V_T distribution due to MGW variability for different grain sizes at V_D=0.6 V. The theoretical quantiles from the normal distribution are also represented (black dashed lines). For small metal grain sizes [see Fig. 9(b), the case GS=3 nm], V_T approximates to a Gaussian distribution. Note that for this case the plot is close to be linear. An increase in the grain size leads to an increasing deviation of the Gaussian behaviour in the tails due to the bounded nature of the distribution.

Fig. 6 shows the DIBL variation as a function of V_{Tlow} and V_{Thigh} due to MGW at two different grain sizes: 10 nm (bottom figure in the left) and 3 nm (bottom figure in the right). The DIBL shows very strong negative correlations with the threshold voltage, that are slightly larger for the 3 nm grain size (CC are -0.89 and -0.94 with V_{Tlow} and V_{Thigh}) than for the 10 nm one (CC are -0.83 and -0.9 with V_{Tlow} and V_{Thigh}). The correlation of the V_T is stronger for the MGW than for the other analysed sources of variability. The DIBL standard deviation is also larger for the MGW variability (36 mV/V for

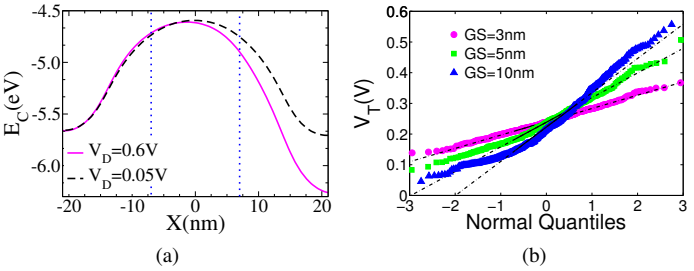


Fig. 9. (a) Source to drain conduction band profiles along the middle of the III-V FinFET device at V_G=V_T. The gate is enclosed between the blue dot lines. (b) Quantile-quantile plots of the V_T distribution due to MGW variability for three different grain sizes.

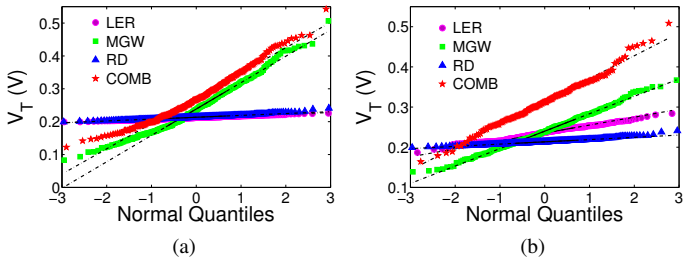


Fig. 10. Quantile-quantile plots of the V_T distribution due to LER, MGW, RD and the combined (LER+MGW+RD) variability for Λ=10 nm, Δ=1 nm and GS=5 nm (a) and for Λ=20 nm, Δ=3 nm and GS=3 nm (b).

GS=10 nm), since the drain field decreases the channel barrier in the end closer to the drain [see Fig. 9(a)], and it will be affected by surface potential variation.

For the WN gate, the MGW variability is the dominant source of fluctuations in III-V FinFETs as compared to RDs and LER. The MGW variability (for a GS=10 nm) induced V_T standard deviations can be up to 17 times larger than the RD and LER (when Λ=10 nm and Δ=1 nm) fluctuation values.

D. Combined RD, LER and MGW variability

Finally, we have analysed the overall variability at a high drain bias when the three sources of fluctuations (RD+LER+MGW) are included at the same time. We have selected two variability-source parameter combinations: i) Λ=10 nm, Δ=1 nm and GS=5 nm (minimum LER and an intermediate MGW case, to avoid masking completely the effect of the other two sources of variability), and ii) Λ=20 nm, Δ=3 nm and GS=3 nm (maximum LER and minimum MGW observed standard deviations).

Figs. 10(a) and (b) show the normal Q-Q plots of the V_T distribution due to the combined RD+LER+MGW variability for cases i) and ii), respectively. The combined V_T spread for case i) is 74 mV and the induced V_{Tshift} is 75 mV. For this combination, the results are completely controlled by the MGW, and there is a negligible influence from the other sources of variability. In Fig. 10(a), both the MGW and the combined case i) have a similar slope and they are just shifted versions of each other. However, in Fig. 10(b) there is a noticeable influence of the LER variability leading to a larger change both in the slope and the V_{Tshift} value for the case ii). The combined standard deviation and shift in the threshold

voltage for this case are 57.2 mV and 113 mV, respectively. These values are much larger than the statistical sum of the three quantities.

IV. Conclusion

We have presented a statistical analysis of three sources of intrinsic parameter fluctuations, RD, LER and MGW, affecting a 14 nm gate length III-V FinFET. We have analysed the influence of four figures of merit influencing the sub–threshold region: subthreshold slope, threshold voltage, off–current and drain-induced-barrier-lowering at both low and high drain biases. The simulations have been performed using our 3D drift–diffusion simulation approach for III–V materials that incorporates i) Fermi-Dirac statistics to accurately model heavily doped source/drain and ii) quantum corrections using the density gradient approach to mimic the effect of quantum confinement. We have found a dramatic reduction in the RD statistical variability, $\sigma V_T = 6$ mV, when compared to planar bulk MOSFETs, and a very similar value to that observed in equivalent gate length FinFETs on SOI substrate. The LER induced variations are very small and similar in magnitude to the RD fluctuations when Δ=1 nm. For larger Δs, the LER variability increases, showing spreads in V_T of up to 19 mV, which is significantly smaller than the variability reported for the 13 nm Si FinFETs [19]. The MGW variability is a dominant source of fluctuations, having a considerable impact on the device characteristics. For the 10 nm grain size, σV_T is over 100 mV, a much larger value than that in SOI FinFETs (σV_T around 40 mV) [10].

To conclude, the variability due to RD and LER in InGaAs FinFETs is comparable or smaller than in the corresponding Si devices, as also observed in [11]. However, the use of WN as a metal gate for the InGaAs FinFETs gives extremely large MGW variability in the device characteristics. This is due to the span of 1.0 eV in the workfunctions of the different grain orientations, much larger than that of TiN, used in Si FinFETs (0.2 eV). Therefore, the WN metal gate looks unsuitable for application in III-V FinFETs.

References

[1] J. Gu, Y. Liu, Y. Wu, R. Colby, R. G. Gordon and P. D. Ye, "First experimental demonstration of gate-all-around III-V MOSFETs by top-down approach", *IEDM Tech. Dig.*, pp. 769-772, 2011.

[2] F. Xue, A. Jiang, Y-T. Chen, Y. Wang, F. Zhou, Y-F. Chang and J. Lee,"Excellent device performance of 3D $In_{0.53}Ga_{0.47}As$ gate-wrap-around field-effect-transistors with high-k gate dielectrics", *IEDM Tech. Dig.*, pp. 629-632, 2012.

[3] K. Kalna, N. Seoane, A. J. Garcia-Loureiro, I. G. Thayne, and A. Asenov, "Benchmarking of scaled InGaAs implant free NanoMOSFETs", *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2297-2306, 2008.

[4] K. Kalna, L. Yang, and A. Asenov, "Monte Carlo simulations of sub-100 nm InGaAs MOSFETs for digital applications", in Proc. ESSDERC 2005, ed. by G. Ghibaudo, T. Skotnicki, S. Cristoloveanu and M. Brillouët, Grenoble, France, pp. 169-172, 2005.

[5] M. Bohr, "The evolution of scaling from the homogeneous era to the heterogeneous era", *IEDM Tech. Dig.*, pp. 1-6, 2011.

[6] K. J. Kuhn, M. D. Giles, D. Becher, P. Kolar, A. Kornfeld, R. Kotlyar, S. T. Ma, A. Maheshwari and S. Mudanai , "Process technology variation", *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 21972208, Aug. 2011.

[7] N. Seoane, M. Aldegunde, A. J. Garcia-Loureiro, R. Valin, and K. Kalna, "3D 'atomistic' simulations of dopant induced variability in nanoscale implant free $In_{0.75}Ga_{0.25}As$ MOSFETs", *Solid-St. Electron.*, vol. 69, pp. 43-49, 2012.

[8] A. Asenov, S. Kaya and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness", *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1254-1259, 2003.

[9] N. Seoane, G. Indalecio, E. Comesaña, A. J. García-Loureiro, M. Aldegunde and K. Kalna, "Three-dimensional simulations of random dopant and metal-gate workfunction variability in an $In_{0.53}Ga_{0.47}As$ GAA MOSFET", *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 205-207, 2013.

[10] X. Wang, A. R. Brown, B. Cheng and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs", *IEDM Tech. Dig.*, pp. 103-106, 2011.

[11] N. Agrawal, Y. Kimura, R. Arghavani and S. Datta, "Impact of transistor architecture (bulk planar, trigate on bulk, ultrathin-body planar SOI) and material (silicon or III-V semiconductor) on variation for logic and SRAM applications", *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3298-3304, 2013.

[12] M. G. Ancona and G. J. Iafrate, "Quantum correction to the equation of state of an electron gas in a semiconductor", *Phys. Rev. B*, vol. 39, no. 13, pp. 9536-9540, 1989.

[13] International Technology Roadmap for Semiconductors (ITRS), 2011 Edition, http://www.itrs.net/Links/2011ITRS/Home2011.htm

[14] A. J. Garcia-Loureiro, N. Seoane, M. Aldegunde, R. Valin, A. Asenov, A. Martinez and K. Kalna, "Implementation of the density gradient quantum corrections for 3D simulations of multigate nanoscaled transistors", *IEEE Trans. Comput-Aided Des. Integr. Circuits Syst.*, vol. 30, no. 6, pp. 841-851, 2011.

[15] A. Islam and K. Kalna, "Monte Carlo simulations of mobility in doped GaAs using self-consistent Fermi-Dirac statistics", *Semicond. Sci. Technol.*, vol. 26, No. 5, 055007 (9pp), 2011.

[16] ATLAS Users Manual, Silvaco Inc., pp. 13-1-24, 2012.

[17] A. Asenov, J.R. Waitling D.K. Ferry and A.R. Brown,"The use of quantum potentials for confinement and tunnelling in semiconductor devices", *J. Comput. Electron.*, vol. 1, pp. 503-513, 2002.

[18] A. Dixit, K. G. Anil, E. Baravelli, P. Roussel, A. Mercha, C. Gustin, M. Bamal, E. Grossar, R. Rooyackers, E. Augendre, M. Jurczak, S. Biesemans, and K. D. Meyer, "Impact of stochastic mismatch on measured SRAM performance of FinFETs with resist/spacer-defined fins: Role of line-edge-roughness", *IEDM Tech. Dig.*, pp. 709-712, 2006.

[19] G. Leung and C. O. Chui, "Variability of inversion-mode and junction-less FinFETs due to line edge roughness", *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1489-1491, 2011.

[20] H. F. Dadgour, K. Endo, V. K. De and K. Banerjee, "Grain-orientation induced work function variation in nanoscale metal-gate transistors–Part I: modeling, analysis, and experimental validation", *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2504-2514, 2010.

[21] H. F. Dadgour, K. Endo, V. K. De and K. Banerjee, "Grain-orientation induced work function variation in nanoscale metal-gate transistors–Part II: implications for process, device, and circuit design ", *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2515-2525, 2010.

[22] S. Agarwal, R. K. Pandey, J. B. Johnson, A. Dixit, M. Bajaj, S. S. Furkay, P. J. Oldiges, K. V. R. M. Murali, "Ab initio Study of Metal Grain Orientation-Dependent Work Function and its Impact on FinFET Variability", *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2728-2733, 2013.

[23] G. Indalecio, A. J. Garcia-Loureiro, M. Aldegunde, and K. Kalna, "3D simulation study of work-function variability in a 25 nm metal-gate FinFET with curved geometry using Voronoi grains", in *Proc. 17th Int. Conf. Simul. Semicond. Proc. Devices (SISPAD)*, pp. 149-152, 2012.

[24] S. H. Rasouli, K. Endo, and K. Banerjee, "Work-Function variation induced fluctuation in bias-temperature-instability characteristics of emerging metal-gate devices and implications for digital design", in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 714-720, 2010.