An 11 mA Capacitor-Less LDO With 3.08 nA Quiescent Current and SSF-Based Adaptive Biasing

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***Abstract*—This brief presents an ultra-low power low-dropout (LDO) regulator with an experimental total quiescent current consumption of only 3.08 nA. The circuit is designed to operate with a load current in the range 0 - 11 mA. A novel adaptive biasing scheme based on a super source follower (SSF) structure is proposed, which measures the absolute voltage difference between the two inputs of the LDO's error amplifier and modifies the biasing current accordingly. Thus, the transient response of the regulator is improved by counteracting the effect of using such a low bias current. The proposed LDO has been fabricated in a standard CMOS 180 nm process and the experimental characterization showed an outstanding performance in terms of maximum load current over quiescent current consumption ratio.**

***Index Terms*—Adaptive biasing, analog integrated circuits, capacitor-less LDO, low-power, nano-ampere, super source follower.**

I. Introduction

LOW POWER voltage regulators are of paramount importance in many power management systems, particularly in the context of the Internet of Things (IoT) and wearable or implantable devices for biomedical applications, [1], [2]. This constraint is even more critical for those systems relying on micro energy harvesting power supply, where the available power is in the μW level at most [3]–[5].

Among voltage regulators, LDO implementations consisting of an error amplifier (EA), a pass transistor, M_{pass}, and a passive feedback network constitute one of the most popular solutions, [6]–[10]. The output voltage of the LDO depends on a reference voltage, V_{ref}, and it can be adjusted by choosing the feedback factor. On the other hand, the driving capability of the LDO relies on both the dimensions and the maximum achievable source-gate voltage of the pass transistor. In typical applications, the load current shows a variation range of several orders of magnitude, from nA to mA, thus requiring a large aspect ratio for M_{pass}. At the same time, a fast load transient response with a reduced power consumption in the standby operation is desirable. In order to meet these requirements, the design trade-off imposed by a low quiescent current and a high drive capability must be considered.

Previous works report the use of super source follower (SSF) structures at the LDO output stage in order to boost the driving capability of the pass transistor, [11], [12], or to optimize the stability [13], [14]. In this work, we propose an alternative scheme consisting of a SSF-based structure, which, to the best of our knowledge, has not been previously proposed in the literature, to perform an adaptive biasing of the EA. The underlying idea is to measure the voltage difference between the two inputs of the EA and to generate a biasing current proportional to the measured difference. In so doing, the quiescent current consumption is kept low when the load current of the regulator remains constant, whereas high driving capability of the EA and fast response, always considering the extremely low value of the quiescent current available, are achieved at sudden changes of the load current.

The brief is organized as follows. In Section II the operation principle of the adaptive biasing is presented, while Section III deals with the implementation of the overall LDO and simulation characterization. Section IV provides experimental results of 14 fabricated samples in TSMC 180 nm CMOS technology. Finally, conclusions are drawn in Section V.

II. SSF Voltage Difference Meter

The SSF is an improved voltage follower including a feedback loop that leads to a reduction of the effective output impedance of the circuit [15]. Besides, the feedback action, established by an additional transistor with respect to the conventional implementation, allows a high-drive current capability in one direction, sourcing or sinking, depending on the type of transistor involved. The composite structure in Fig. 1 incorporates two SSF cells (in red), each consisting of two driver transistors and two current sources. The output voltage of each SSF in Fig. 1, $V_{o1(2)}$, depends on the aspect ratio of transistors $M_{i1(2)}$, which are selected to be equal, and on their biasing current, I_{bias1}. Indeed, these factors determine the gate-to-source voltage $V_{i1(2)} - V_{o1(2)}$ of $M_{i1(2)}$. Thus, the output voltage of the SSF is given by (1), where $\Delta V_{1(2)}$ is the gate-to-source voltage of $M_{i1(2)}$, described in (2) by an equation valid for all operating regions, i.e., weak, moderate

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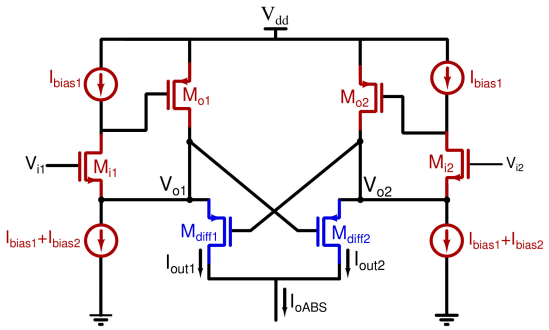


Fig. 1. SSF AVDM circuit.

and strong inversion [16]. In (2), V_{thn} is the threshold voltage of $M_{i1(2)}$, and $I_{sn} = 2n_n\mu_n C_{ox}V_T^2$ is the characteristic current being μ_n the electron mobility, C_{ox} the gate capacitance, n_n the NMOS subthreshold slope factor and V_T the thermal potential.

$$V_{o1(2)} = V_{i1(2)} - \Delta V_{1(2)} \tag{1}$$

$$\Delta V_{1(2)} = V_{thn} + 2n_n V_T ln\left(e^{\sqrt{\frac{I_{bias1}}{I_{sn}\frac{W_{i1(2)}}{L_{i1(2)}}}}} - 1\right) \tag{2}$$

The maximum output current that the SSF can deliver, $I_{out1(2)max}$, is determined by the drive capability of transistor $M_{o1(2)}$, which relies on its size, $W_{o1(2)}/L_{o1(2)}$, and its maximum source-to-gate voltage $V_{sgo1(2)}$. Indeed $V_{sgo1(2)}$ sets the drain voltage, $V_{di1(2)}$, of transistor $M_{i1(2)}$ and its maximum value is limited by the operation of these transistors in saturation. Assuming transistor $M_{o1(2)}$ operating in strong inversion at the maximum output current in the SSF, $I_{out1(2)_{max}}$, takes the form of (3), where μ_p is the hole mobility, V_{thp} the threshold voltage of the PMOS transistors and $V_{di1(2)_{min}}$ is given by (4) [16].

$$I_{out1(2)_{max}} = \frac{1}{2}\mu_p C_{ox}\frac{W_{o1(2)}}{L_{o1(2)}}(V_{dd} - V_{di1(2)_{min}} + V_{thp})^2 - I_{bias2} \tag{3}$$

$$V_{di1(2)_{min}} = V_{i1(2)} - \Delta V_{1(2)} + 2V_T\sqrt{\frac{I_{bias1}}{I_{sn}\frac{W_{i1(2)}}{L_{i1(2)}}} + 0.25} + 3V_T \tag{4}$$

Adding the PMOS transistor $M_{diff1(2)}$ to the SSF, colored in blue in Fig. 1, the SSF can be used to compare two voltages, in this case V_{o1} and V_{o2}. As a result, an output current $I_{out1(2)}$ is obtained, which depends on the voltage difference $V_{o1(2)} - V_{o2(1)}$, as shown in (5), where $I_{sp} = 2n_p\mu_p C_{ox}V_T^2$ being n_p the PMOS subthreshold slope factor.

$$I_{out1(2)} = I_{sp}\frac{W_{diff1(2)}}{L_{diff1(2)}}\left[ln\left(1 + e^{\frac{V_{o1(2)} - V_{o2(1)} + V_{thp}}{2n_p V_T}}\right)\right]^2 \tag{5}$$

To generate an output current that depends on the absolute difference between two voltages, two mirrored SSF acting as voltage difference meters must be used as shown in Fig. 1. In so doing, two shifted values of the input voltages, V_{o1} and V_{o2}, are compared, and so are indirectly V_{i1} and V_{i2}, building the absolute voltage difference meter (AVDM). Applying (1), (2) and (5) to the AVDM, equation (6) is obtained assuming $M_{i1} = M_{i2}$, $M_{o1} = M_{o2}$ and $M_{diff1} = M_{diff2}$ and being $\Delta_{21} = V_{i2} - V_{i1} + V_{thp}$ and $\Delta_{12} = V_{i1} - V_{i2} + V_{thp}$.

$$I_{oABS} = I_{sp}\frac{W_{diff}}{L_{diff}}\left[\left(ln\left(1 + e^{\frac{\Delta_{21}}{2n_p V_T}}\right)\right)^2 + \left(ln\left(1 + e^{\frac{\Delta_{12}}{2n_p V_T}}\right)\right)^2\right] \tag{6}$$

When $V_{i1} = V_{i2}$, the output current of the AVDM falls to its lowest value, which can be calculated using (7) resulting from simplifying (6) making $\Delta_{12} = \Delta_{21} = V_{thp}$ and using the approximation $ln(1 + a) \approx a$ when $a << 1$.

$$I_{oABS}|_{V_{i1}=V_{i2}} \simeq 2 \times I_{sp}\frac{W_{diff}}{L_{diff}}e^{\frac{V_{thp}}{n_p V_T}}. \tag{7}$$

III. Low-Power LDO With Adaptive Biasing EA

The transient response of an LDO depends on the driving capability of the pass transistor and, hence, on the EA maximum output current. When subjected to rapid changes in the load current, the variations on the output voltage of the LDO will make EA inputs unequal. Thus, to provide a fast response without increasing the quiescent power consumption, an EA with a high output current during transient episodes, for a quick charge/discharge of the pass transistor gate node, but with a reduced biasing current in the steady state, is needed.

Fig. 2 shows the schematic of the proposed adaptively biased LDO composed of (from left to right): i) an SSF AVDM circuit, ii) a section to determine the biasing point of the amplifier, iii) a PMOS input differential amplifier, and iv) a pass transistor, M_{pass}, and four diode-connected PMOS transistors, M_{div1-4}, working as a resistor divider to determine the feedback voltage V_{fb}. The reason for using active devices in the feedback network is the difficulty of implementing a large resistor on-chip in order to limit the divider current in the pA order. In the AVDM section, transistors $M_{biasSSF}$, M_{PbSSF} and M_{NbSSF} set the SSFs' biasing currents from an external bias current, $I_{biasSSF}$, by means of the current mirrors $M_{biasSSF} - M_{PSSF+,PSSF-}$ and $M_{NbSSF} - M_{NSSF+,NSSF-}$. The output current of the AVDM, I_{oABS}, is mirrored by $M_{absdiff}$ into M_{mirror} by means of its gate voltage V_Δ. In the biasing circuit, the ratio $M_{absdiff}$:M_{mirror} sets the bias current of the EA, $I_{biasAMP}$, from I_{oABS}. This current is then mirrored to M_{Pb2}, generating the voltages V_{bias1} and V_{bias2} that bias the cascode stage, and to M_{pinamp} , which provides the tail current to the differential pair M_{Pi+}, M_{Pi-}, respectively. The working principle of the adaptive biasing scheme is based on the fact that under sudden variations of the load current, the input voltages of the EA, V_{fb} and V_{ref} will have different values and the currents I_{oABS} and $I_{biasAMP}$ will increase significantly. This will allow in such a case the EA to provide larger output currents to charge/discharge its output node and, consequently, drive faster the pass transistor gate voltage, while keeping a low quiescent current under steady load conditions.

The AVDM has been designed to work in the subthreshold region, with a biasing current, $I_{biasSSF}$, as low as 100 pA. Besides, transistors M_{oSSF+} and M_{oSSF-} have a small W/L ratio to limit the maximum output current of the AVDM.

A. Stability of the Proposed Regulator

Due to the low biasing current of the EA at the steady state of the regulator, the dominant pole of the system will be

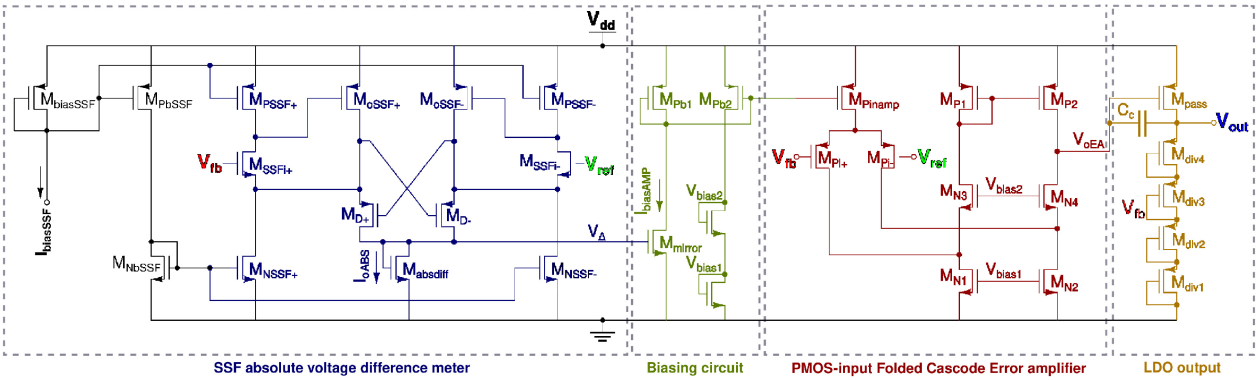


Fig. 2. Proposed adaptively biased error amplifier LDO.

located at the EA's output, node V_{oEA}. The worst-case scenario in terms of stability of the system will occur for the minimum load current with a high load capacitor, as in this case the pole at the output of the voltage regulator will be set at its minimum frequency, approaching the unity gain frequency.

Equations (8) and (9) show the pass transistor's gate pole and the output node pole respectively, where A_{EA} is the gain of the error amplifier, that can be calculated using (10), and A_{pass} is the gain of the pass transistor expressed as (11). The gain of the loop will be $A_{loop} = \beta A_{EA} A_{pass}$ where β is the feedback factor determined by the resistor divider, which has a value $\beta = 0.5$ in the proposed implementation.

In order to avoid stability issues, a compensation capacitor, C_c, was used to ensure that both poles are far enough from each other. The stability criterion considered in this case was to set the output pole at a frequency at least 1.5 times the unity gain frequency of the loop with the aim of obtaining a phase margin of 60°, mathematically expressed as (12).

$$p_{oEA} \approx \frac{-g_{oEA}}{(1 - A_{pass})(C_c + C_{gdpass})} \tag{8}$$

$$p_{out} \approx -\frac{g_{mpass}}{C_L} \tag{9}$$

$$A_{EA} \approx \frac{g_{mpiEA}}{g_{oEA}} \tag{10}$$

$$A_{pass} \approx \frac{-g_{mpass}}{g_L + g_{div} + g_{dspass}} \tag{11}$$

$$|p_{out}| > 1.5 \times |p_{oEA} \cdot \frac{A_{pass} A_{EA}}{2} \cdot 10^{\frac{-3}{20}}| \tag{12}$$

$$C_{c,min} \approx 0.531 \cdot \frac{g_{mpiEA}}{g_{mpass}} \cdot C_L - C_{gdpass} \tag{13}$$

Applying (12) for a load capacitance of $C_L = 10$ pF, the calculated value of the compensation capacitor that ensures stability at zero load current, calculated according to (13), is $C_c \approx 75$ fF. The implemented value in the fabricated prototypes was $C_c = 77$ fF. To check the robustness of the compensation scheme, simulations varying C_L, I_L and across PVT corners were run. In the typical mean simulation, the phase margin takes a value of 65° when $I_L = 0$ and $C_L = 10$ pF, decreasing to 45° when $I_L = 0$ and $C_L = 30$ pF. The PVT analysis varying the temperature in the range 0-80 °C and the input voltage ±10%, led to a worst-case phase margin of 20° for the *sf* corner, 60 °C, and $I_L = 0$. Nevertheless, in a realistic implementation, the load current will probably be

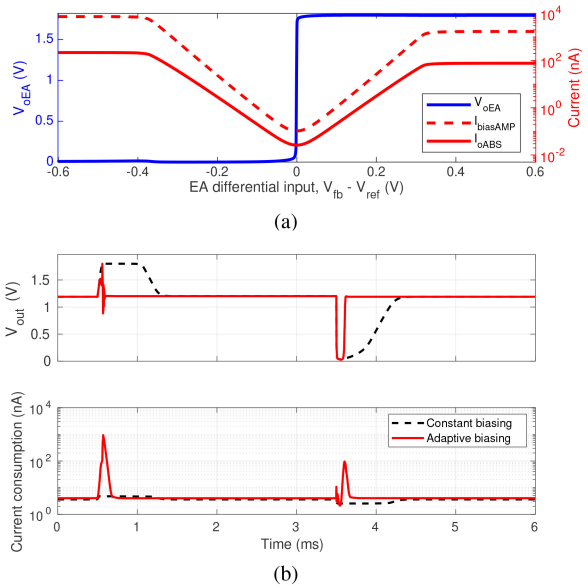
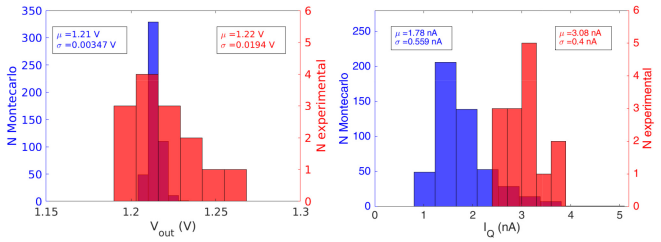


Fig. 3. Simulation results of (a) the error amplifier and (b) transient response comparison between a constant biased and proposed adaptively biased EA in an LDO.

at least in the order of nA. Repeating the PVT analysis for $I_L = 100$ nA, the lowest phase margin raised up to 38°.

B. Simulation Results

DC simulation results of the proposed adaptively biased EA, shown in Fig. 3(a), exhibit that the biasing current of the amplifier, $I_{biasAMP}$, varies between a minimum value of 105 pA when both inputs, V_{fb} and V_{ref} in Fig. 2, are equal, and a maximum value of 7.3 μA for high input differences. This current is multiple of the output of the AVDM, I_{oABS}, which follows the behaviour predicted by equation (6). At the same time, the EA output voltage shows a DC gain of 692 V/V, equivalent to 56.8 dB. A simulated comparison between the responses of the proposed LDO including the adaptively biased EA proposed and an EA with fixed biasing current, both with the same nominal value of quiescent current $I_Q \simeq 3.5$ nA, was also carried out and is shown in Fig. 3(b). The simulation results show a transient response improvement of 14×, from 1.72 ms to 0.12 ms, for a step-up current transition from 120 nA to 11.1 mA and of 8×, from 2.05 ms to 0.25 ms, for the step-down current transition when using the proposed amplifier instead of



(a) (b)

Fig. 4. Distributions of a 500-run Montecarlo analysis and experimental data for (a) V_{out} and (b) I_Q.

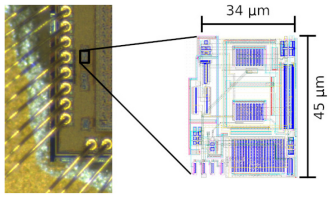


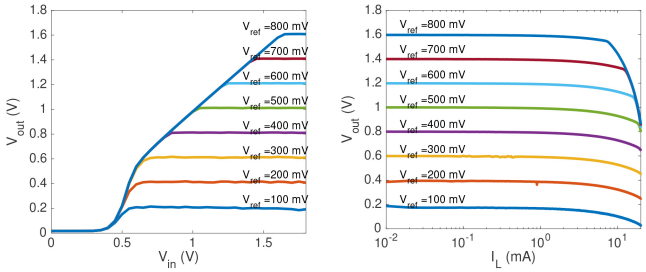
Fig. 5. Chip microphotography and layout capture.

a constant biased scheme. The AVDM circuit shows a delay at each transition event, which could be decreased by using a larger $I_{biasSSF}$, even though in our implementation we have decided to keep current consumption as low as possible. The Fig. 4(a) and the Fig. 4(b) show, in blue color, Montecarlo simulations to evidence the expected dispersion due to mismatch and process variations when $V_{dd} = 1.8$ V and $V_{ref} = 600$ mV. As it can be seen, the quiescent current consumption displays a spread around the mean value ascribed to the exponential dependence of the subthreshold current with the threshold voltage dispersion. In any case, the expected quiescent current consumption in the worst case remains below 5 nA.

IV. Experimental Results

The proposed LDO was fabricated in standard TSMC 180 nm CMOS technology. A microphotograph of the chip highlighting the layout dimensions and the position of the LDO circuit is shown in Fig. 5. A total of 14 samples have been characterized with an experimental setup that included a Tektronix MDO4034C oscilloscope, a Keithley 6487 picoammeter, a NI USB-6341 DAQ and a Keithley 2450 SMU. The biasing current $I_{biasSSF} = 100$ pA was generated on-chip by means of a current divider which by Montecarlo simulation offers a maximum dispersion of $\pm 3\%$ from the expected nominal value.

For the experimental determination of the output voltage and the quiescent current consumption, values of $V_{dd} = 1.8$ V and $V_{ref} = 600$ mV, which lead to $V_{out} = 1.2$ V (in the absence of load current, I_L), were considered, and the measured histograms are shown in red color in the Figs. 4(a) and 4(b). The experimental I_Q distribution gives an average value of only 3.08 ± 0.40 nA, being, to the best of our knowledge, the lowest reported in the literature [17], [21]. Preliminary results in [23] showed a similar value of roughly 2 nA, but the chip contained structural failures that have been solved in the present implementation. With respect to the line sensitivity (LS), shown in Fig. 6(a) for a load resistance of 1.5 kΩ, it has a value LS $= 0.71 \pm 0.42$ mV/V, whereas for the load regulation, shown in Fig. 6(b), a value LR $= -8.66 \pm 2.16$ mV/mA was obtained.



(a) (b)

Fig. 6. Measured output voltage of the regulator for several reference voltages varying (a) V_{in} and (b) I_L.

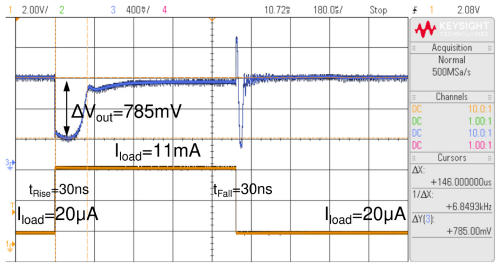


Fig. 7. Experimental transient response of the proposed LDO.

In the latter case, at least 4 mV/mA can be attributed to the metal lines connecting to the output pads according to the data provided by the foundry. The results shown in Fig. 6 underline the flexibility of the proposal, able to work with a wide range of power supplies, reference voltages and load currents. The values chosen for our particular application case were $V_{dd} = 1.8$ V, $V_{ref} = 600$ mV and $I_L = 11$ mA.

The transient response of the proposed adaptively biased LDO when I_L is changed from 20 μA to 11 mA with an edge time of 30 ns is shown in Fig. 7. As can be seen, the settling time was $t_{s,up} = 147$ μs for the step-up load current pulse and $t_{s,down} = 82$ μs in the step-down load current transition. The relatively large undershoot is in line with other very low I_Q LDOs in the literature [17], [24]. In applications in which certain basic building blocks present a self-startup behaviour, such as a micro-energy harvester, the illustrated voltage variation is not a major issue. With respect to the power supply rejection, the observed behaviour has the conventional response of an LDO when no ad hoc circuit for PSR improvement is included [18], [20], [25]. The measured PSR is -40 dB @ 10 Hz when $I_L = 0$, -38 dB @ 10 Hz with $I_L = 11.1$ mA, -2.3 dB @ 10 kHz with $I_L = 0$ and -5.2 dB @ 10 kHz when $I_L = 11.1$ mA. Using the relation $PSR_{s=0} \simeq LS$ [7], the PSR at DC can be specified as -63 dB.

A summary of the main experimental results of the proposed circuit can be found in Table I, together with a comparison with the only state-of-the-art regulators with nanoampere range quiescent current consumption found in the literature. As can be seen, our approach achieves the lowest I_Q of the comparative with similar or slightly higher maximum I_L. The figures of merit (FoM) considered are the most used in the literature, being defined as $FoM_t = T_R I_Q / \Delta I_L$ [26], where T_R is the response time, and $FoM_v = K \Delta V_{out} I_Q / \Delta I_L$ [27], where K is the time-edge ratio calculated by dividing the current edge time of each contribution by the fastest current edge time in the comparative, and ΔV_{out} and ΔI_L are the voltage drop and

TABLE I
SUMMARY OF THE EXPERIMENTAL RESULTS AND STATE-OF-THE-ART COMPARISON

	This work	TCASI'18 [17]	TCASII'18 [18]	TCASII'19 [19]	ACCESS'19 [20]	JSSC'20 [21]	ISCAS'21 [22]
Technology	180 nm	65 nm	180 nm	180 nm	65 nm	55 nm	180 nm
Capacitor-less	yes	yes	yes	yes	yes	no	yes
Size (μm^2)	1530	4200	210000	31000	7000	42000	128000
I_Q (nA)	3.08	30	133000	10800	9600	16	11
I_L max (mA)	11	10	50	100	70	10	50
LS (mV/V)	0.71	-	2.67	10	3.84	0.5	0.86
LR (mV/mA)	8.62	1.22	0.194	0.081	0.29	1.05	0.2
PSR@10 Hz (dB)	-40@0 mA -38@11.1 mA	-	-	-	-67‡ @heavy load	-75@1 nA -43@10 mA	-
PSR @ 10 kHz (dB)	-2.3@0 A -5.2@11.1 mA	-40@10.3 mA	-70@50 mA	-	-26‡ @heavy load	-100@1 nA -43@10 mA	-
FoM_t (ps)	41	0.75†	50.54	22.4	247	11.4	582
k*	85.7	571	1	286	-	57	-
FoM_v (μV)	19	836	441	5892	-	6.4	-

† Estimated from the transient response. ‡ Simulation result. $k^* = \frac{I_L \text{ edge time}}{\text{Shortest edge of the comparative}}$

the load current variation, respectively. Our implementation shows a FoM_t higher as compared to the other approaches and a FoM_v between them. Indeed, the design emphasis was made in maintaining I_Q very low and independent of I_L, rather than in reducing the response time. If a speed up of the transient response is desired, the biasing current $I_{biasSSF}$ can be raised to make the AVDM circuit faster, thus improving the transient response of the overall LDO and reducing the FoM_t. Furthermore, our implementation keeps the quiescent current consumption roughly constant regardless of the load current, unlike [17], [21] and [22] where I_Q depends on I_L to a greater or lesser degree.

V. CONCLUSION

A capacitor-less ultra-low power LDO is presented in this brief using a novel AVDM structure to measure absolute voltage differences based on a SSF. This AVDM was used to implement an adaptive biasing scheme of the error amplifier in order to improve the transient response of the regulator under sudden changes of the load current. The experimental characterization shows settling times in the order of 150 μs with the lowest quiescent current reported in the literature.

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