Comparison of Fin Edge Roughness and Metal Grain Work Function Variability in InGaAs and Si FinFETs

N. Seoane, G. Indalecio, M. Aldegunde, D. Nagy, M. A. Elmessary, A. J. García-Loureiro and K. Kalna

***Abstract*—The fin edge roughness (FER) and the TiN metal grain work-function (MGW) induced variability affecting off and on device characteristics is studied and compared between a 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET and a 10.7 nm gate length Si FinFET. We have analysed the impact of variability by assessing five figures of merit (V_T, SS, I_{OFF}, DIBL and I_{ON}) using two state-of-the-art in-house-build 3-D simulation tools based on the finite element method. Quantum-corrected 3-D drift-diffusion simulations are employed for variability studies in the sub-threshold region while, in the on-region, we use quantum-corrected 3-D ensemble Monte Carlo simulations. The $In_{0.53}Ga_{0.47}As$ FinFET is more resilient to the FER and MGW variability in the sub-threshold compared to the Si FinFET due to a stronger quantum carrier confinement present in the $In_{0.53}Ga_{0.47}As$ channel. However, the on-current variability is between 1.1-2.2 times larger for the $In_{0.53}Ga_{0.47}As$ FinFET than for the Si counterpart, respectively.**

***Index Terms*—Intrinsic parameter fluctuations, fin-edge roughness, gate work function variability, Si, III-V materials, FinFETs.**

I. Introduction

NON-PLANAR multi-gate transistors like FinFETs are leading solutions for the future sub-14 nm digital technology [1]. To meet the ITRS requirements, the future multi-gate transistors may use III-V channel materials which are intensively researched as a possible replacement for *n*-type Si channels because of their higher electron mobility and saturation velocity [2]. These further scaled solutions require not only a realistic assessment of their performance, which is strongly affected by the exact device geometry and design, but also the determination of how different sources of device variability can affect characteristics and reliability.

Variability of transistor characteristics is not only a problem that mainly affects the device fabrication process but it has become an universal concern affecting CMOS and SRAM [3] scaling and perturbing digital logic circuits [4]. New design processes are require to incorporate this phenomena at every level [5]. Nowadays, variability is the main factor restricting the scaling of the supply voltage which, in turn, can lead to unacceptable power dissipation. Random sources of variability such as random dopant fluctuations, line-edge roughness, and metal gate work-function variations, have become dominant in both Si and III-V channel-based nano-MOSFETs [6], [7], [8].

This work is supported by Spanish Government (TEC2014-59402-JIN, TIN2013-41129-P) and EPSRC (EP/I010084/1). NS, GI and AJGL are with the CITIUS, University of Santiago de Compostela, Spain. E-mail: (natalia.seoane@usc.es). MA, DN, MAE and KK are with the ESDC, Swansea University, United Kingdom. MAE is also with Dept of Mathematics & Engineering Physics, Mansoura University, Egypt

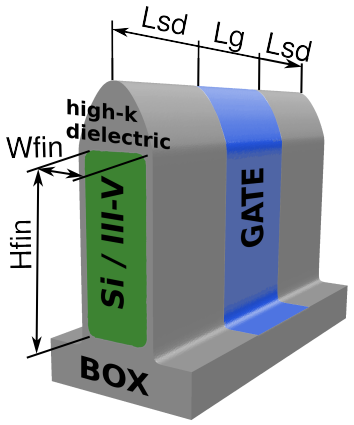

Fig. 1. Schematic structure of the simulated $In_{0.53}Ga_{0.47}As$ and Si FinFETs.

In this work, we have studied and compared the uncorrelated fin-edge roughness (FER) and TiN metal grain work-function (MGW) induced variability in as-close-as-possible $In_{0.53}Ga_{0.47}As$ and Si FinFETs (designed following the ITRS specifications [9]) using state-of-the-art in-house-build 3-D simulation tools. We simulate the variability for device threshold voltage, off-current, sub-threshold slope, drain-induced-barrier-lowering and on-current at both low and high drain biases.

II. FinFET Modelling

The variability study has been performed for a 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET and a 10.7 nm gate length Si FinFET. These devices have been designed following the 2013 ITRS targets for high-performance logic multi-gate devices [9] assuming a *n*-type Gaussian-like doping profile in the source/drain regions (with a N_{SD} peak value) and a *p*-type uniform doping in the channel (N_{ch})[10]. The geometry of the simulated devices is shown in Fig. 1 and their dimensions, doping concentrations and applied drain biases are listed in Table I. The work-function of the TiN metal was set to be 4.52 eV. Table II shows the nominal performance values yield by both FinFET devices. On the one hand, the $In_{0.53}Ga_{0.47}As$ FinFET delivers a larger on-current than the Si device but for the price of increase in leakage current when compared to than observed in the Si FinFET. Therefore, the (I_{ON}/I_{OFF}) ratio, close to $6x10^4$, is similar for the both devices.

TABLE I
DIMENSIONS, DOPING CONCENTRATIONS, AND APPLIED DRAIN BIASES FOR THE SIMULATED $In_{0.53}Ga_{0.47}As$ AND SI FINFETS.

Symbol	$In_{0.53}Ga_{0.47}As$	Si
L_G(nm)	10.4	10.7
EOT(nm)	0.59	0.62
W_{fin}(nm)	6.10	5.80
H_{fin}(nm)	15.2	15.0
L_{SD}(nm)	10.4	10.7
$N_{ch}(cm^{-3})$	10^{17}	10^{15}
$N_{SD}(cm^{-3})$	$5x10^{19}$	10^{20}
V_{Dlin}(V)	0.05	0.05
V_{Dsat}(V)	0.60	0.70
WF(eV)	4.52	4.52

TABLE II
NOMINAL PARAMETERS FOR THE SIMULATED $In_{0.53}Ga_{0.47}As$ AND SI FINFETS.

Symbol	$In_{0.53}Ga_{0.47}As$	Si
V_{Tlin}(V)	0.227	0.227
V_{Tsat}(V)	0.183	0.178
SS(mV/dec)	78	76
DIBL(mV/V)	80	75
$I_{OFF}(\mu A/\mu m)$	0.031	0.027
$I_{ON}(mA/\mu m)$	1.77	1.56
(I_{ON}/I_{OFF}) ratio	$5.7x10^4$	$5.8x10^4$

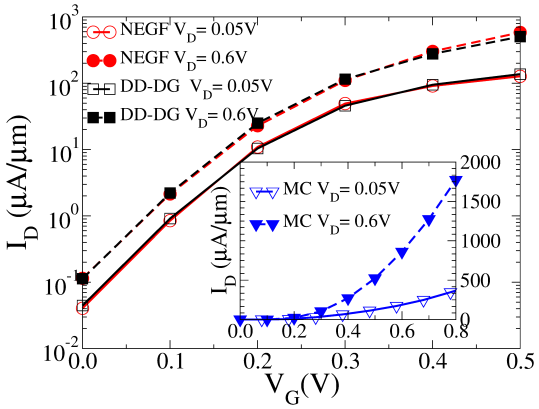

Fig. 2. I_D-V_G characteristics of the 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET comparing 3-D DD-DG to ballistic NEGF simulations [15] in the sub-threshold region. Inset: Monte Carlo (MC) simulations of on-current shown on a linear scale.

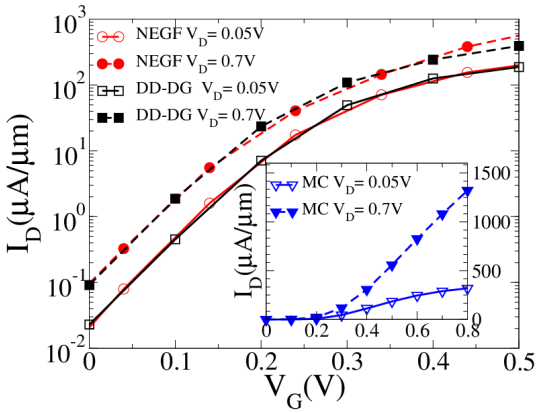

Fig. 3. I_D-V_G characteristics of the 10.7 nm gate length Si FinFET comparing 3-D DD-DG to NEGF simulations with scattering [16] in the sub-threshold region at low and high drain biases. Inset: 3-D Monte Carlo (MC) simulations of on-current shown on a linear scale.

This variability study uses three different simulation tools in a hierarchical workflow from a quantum-transport through a semi-classical to a classical technique. First, we use a 3-D parallel finite-element (FE) drift-diffusion (DD) device simulator [11], [12] with integrated FE density gradient (DG) quantum corrections [13] and Fermi-Dirac statistics [14]. We have calibrated quantum corrections through the effective masses that characterise the DG solution, which mimic the source-to-drain tunnelling and quantum confinement effects [6]. After that, this simulator has been validated at both low and high drain biases against 3-D Non-Equilibrium Green's Functions (NEGF) simulations [15], [16] with an excellent agreement as seen in Figs 2 and 3.

Finally, for studies in the on-region of $In_{0.53}Ga_{0.47}As$ and Si devices, we use a 3-D quantum-corrected FE ensemble Monte Carlo (MC) simulation tool. In the MC simulator, the quantum corrections have been included via the solution of the DG equation for the $In_{0.53}Ga_{0.47}As$ device [10], and of the 2-D Schrödinger equation for the Si device [17], respectively. The MC simulation tool uses an analytic non-parabolic anisotropic model [18] and includes the interface roughness via Ando's model [19]. Note that the 3-D quantum-corrected FE Monte Carlo simulations were verified against experimental I_D-V_G characteristics of a 25 nm gate Si FinFET [10]. The MC considers the following scattering mechanisms: acoustic phonon, non-polar optical intra-valley, non-polar optical inter-valley and ionized impurities (using Ridley's third-body exclusion model [20]). Polar optical phonon, piezoelectric and alloy scattering have also been included for the $In_{0.53}Ga_{0.47}As$ device simulations [21]. The I_D-V_G characteristics of Si and $In_{0.53}Ga_{0.47}As$ FinFETs obtained from the 3-D MC are shown in the insets of Figs 2 and 3 on a linear scale. The channel orientation is $\langle 100 \rangle$. The Γ valley confinement effective mass of $0.083m_0$, deduced from tight-binding calculations for III-V ultra-thin body SOI MOSFETs [22], has been used in the InGaAs FinFETs while the effective masses in the L and X valleys are assumed to be bulk.

III. VARIABILITY COMPARISON BETWEEN SI AND $In_{0.53}Ga_{0.47}As$ FINFETS

We have employed the meticulously calibrated DD-DG simulations to analyse the variability affecting the sub-threshold region of the device comparing four figures of merit: threshold voltage (V_T), sub-threshold slope (SS), off-current (I_{OFF}) and drain-induced-barrier-lowering (DIBL). In the on-region, we have studied the on-current (I_{ON}) variability with the quantum-corrected 3-D FE MC simulation tool. Ensembles of 300 and 100 devices have been used in the analysis of the sub-threshold and on-regions, respectively. To extract the threshold voltage,

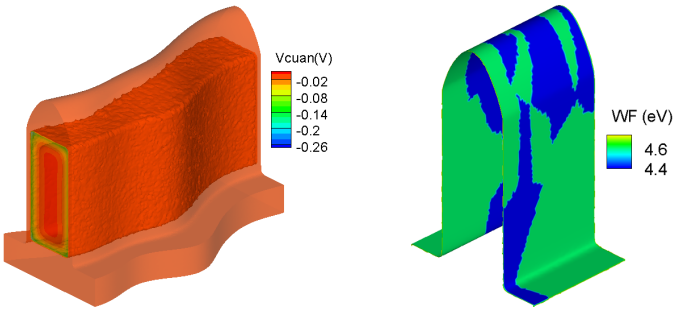

Fig. 4. (Left) Iso-surfaces showing the quantum potential inside a Si FinFET body for a particular fin-edge roughness (FER) profile (CL=20 nm, RMS=1 nm) at V_G=0.92 V and V_D=0.7 V. (Right) Example of a work function distribution in the TiN metal gate due to MGWV for a 5 nm average GS.

we have used the same constant current criterion for both devices ($I_T = 17.56$ A/m). The on-current has been calculated as the drain current when V_G=V_{Dsat}+V_{Tsat} and the off-current has been extracted at $V_G = 0.0$ V.

A. FER and MGW Variability Models

The effect of uncorrelated FER is studied using Fourier synthesis with Gaussian autocorrelation [23]. The FER is implemented as previously described in [6], [24]. DD simulations that include DG quantum confinement corrections have been widely used for the analysis of line-edge-roughness variability [8], [25], [26]. The DG requires calibration which is carried out for ideal nominal device. Once accurately calibrated, the DG quantum corrections will mimic very well the position of the lowest bound state [27]. However, the FER will induce a shift in the ground state, particularly for low mass materials such as InGaAs, which would require small adjustments of DG fitting parameters for each simulated sample [17]. These adjustments, computationally prohibitive in variability studies, would introduce small changes in the carrier density distributions [28].

During the simulations, two values of the correlation length (CL=10 and 20 nm) and three root mean square values (RMS=1, 0.8 and 0.6 nm) are analysed. These values have been chosen in order to represent foreseeable trends required by industry and observed in experiments [7]. Fig. 4 (left) shows an example of the quantum potential inside the Si FinFET body for a particular FER profile (CL=20 nm, RMS=1 nm) at V_G=0.92 V and V_D=0.7 V.

The TiN MGW variability (MGWV) [29] is obtained via the calculation of Voronoi diagrams for a set of randomly generated points which modify the size and shape of the grains. A full description of the followed methodology can be found in [6], [24]. In this work, we analyse four different grain sizes (GSs) (10, 7, 5 and 3 nm) and assume that TiN has two possible grain orientations with MGWs of 4.6 and 4.4 eV and probabilities 60% and 40%, respectively [29]. Fig. 4 (right) shows an example of a particular work-function distribution in the TiN metal gate due to MGWV for a 5 nm average GS.

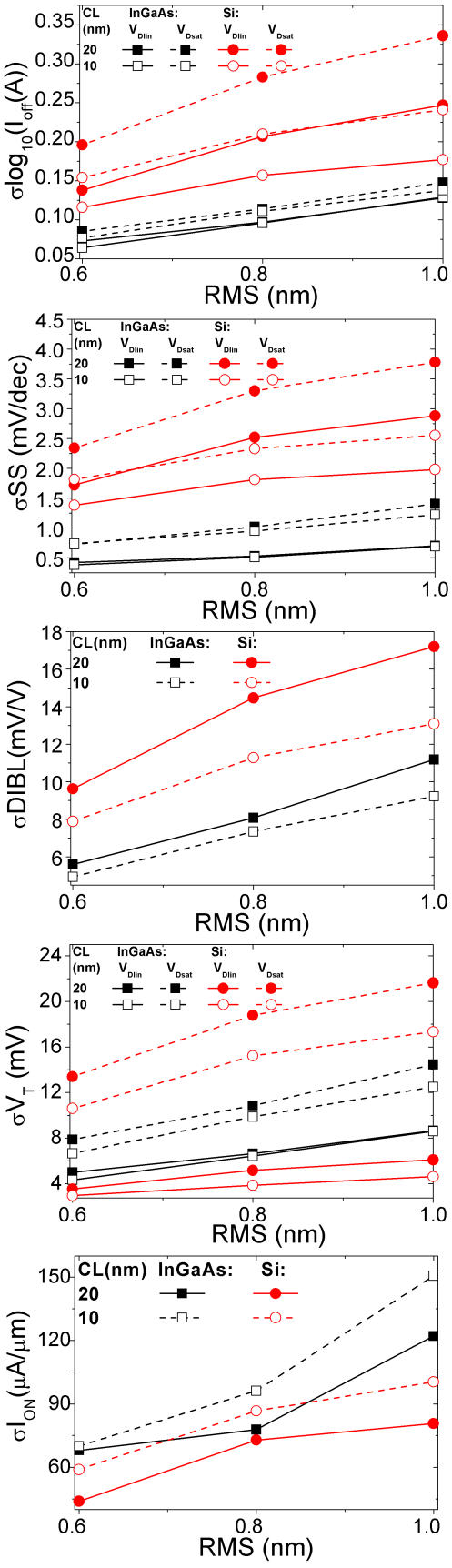

Fig. 5. Comparison of the $\log_{10}(I_{OFF})$, SS, DIBL, V_T and I_{ON} variability due to FER for the studied $In_{0.53}Ga_{0.47}As$ and Si FinFETs at low (V_{Dlin}=0.05 V) and high drain biases ($V_{Dsat} = 0.6$ V and $V_{Dsat} = 0.7$ V, respectively) as a function of the correlation length, and the RMS height.

B. FER Impact on FinFET Variability

Fig. 5 shows a comparison of the $\log_{10}(I_{OFF})$, SS, DIBL, V_T and I_{ON} variability (from the top to the bottom) due to FER for the 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ and 10.7 nm Si FinFETs as a function of the drain bias, the correlation length, and the RMS height.

In the presence of FER, the observed variations for the three figures of merit related to the off-region of the device (I_{OFF}, SS and DIBL) are smaller in the $In_{0.53}Ga_{0.47}As$ FinFET than in the Si FinFET. Note here that the standard deviations for all the figures of merit are strongly affected by the drain bias and the correlation length values in the Si FinFET whereas their impact on the $In_{0.53}Ga_{0.47}As$ FinFET is smaller as previously seen in [6].

We believe that a smaller variability of the $In_{0.53}Ga_{0.47}As$ FinFET compared to the Si device can be understood as follows. In the sub-threshold region, where electrostatics dominates, the variability is governed by the strength of the quantum carrier confinement in the nanoscale channel which is related to the separation of energy levels. The $In_{0.53}Ga_{0.47}As$, being a III-V material, provides a stronger confinement (thanks to a smaller electron effective mass) of electron density in the channel than that in the Si channel [30]. This stronger confinement keeps a large number of carriers in the middle of the channel (a strong body inversion). Thus the carriers in the $In_{0.53}Ga_{0.47}As$ channel will be less affected by disruptions of electrostatics induced by FER leading to a lower variability than the observed in the Si channel. The carriers in the Si channel can spread closer to the FER profile because of the weaker confinement thus interacting with the profile more strongly leading to a larger variability.

On the other hand, we observe that at high drain bias, the FER induced V_T variability is lower for the $In_{0.53}Ga_{0.47}As$ device than for the Si one (same behaviour as in the sub-threshold region magnitudes), while the V_T variability is larger for the $In_{0.53}Ga_{0.47}As$ device than that for the Si one at low drain bias (same behaviour as we will see in the on-region). This opposite behaviour at low and high drain biases is due to the change in the transport regime (V_T is a figure of merit measured at the transition between the off- and on-regions of a device).

In the on-current region, the non-equilibrium carrier transport dominates. We think that the variability will be governed by the efficiency of carrier transport through the channel from the source to the drain and by the gate control of those carriers during the transport process. The $In_{0.53}Ga_{0.47}As$ device has a smaller average effective transport mass when compared to the Si channel providing a faster transport. However, in the on-current regime, the effect of the strong confinement will be less important than in the sub-threshold region. Therefore, these faster III-V carriers with a smaller effective mass interact more strongly with any FER induced electrostatic potential disruptions than the slower carriers with a larger effective mass in Si which leads to a larger variability of the $In_{0.53}Ga_{0.47}As$ transistor.

The I_{ON} variability (the bottom figure of Fig. 5) is between 1.1-1.5 times larger for the $In_{0.53}Ga_{0.47}As$ FinFET than for the Si device. Note that for both devices the variability is larger for a smaller correlation length of 10 nm which is opposite to the behaviour observed in the sub-threshold region. In the on-region, where the conductivity is large, the device shape variations create effective paths for electrons to pass through the channel more easily. This behaviour will happen less frequently for a smaller correlation length since there will be a higher probability of having an uncorrelated variation (both sides of the device will deform towards opposite directions) followed by a correlated one (both sides will deform towards the same direction). For the Si FinFET, when the correlation length is 10 nm, σI_{ON} ranges from 58 μA/μm when RMS=0.6 nm to 105 μA/μm when RMS=1.0 nm. For the same correlation length, the on-current variability $In_{0.53}Ga_{0.47}As$ FinFET is ranging from 69 to 151 μA/μm when the RMS increases from 0.6 to 1.0 nm.

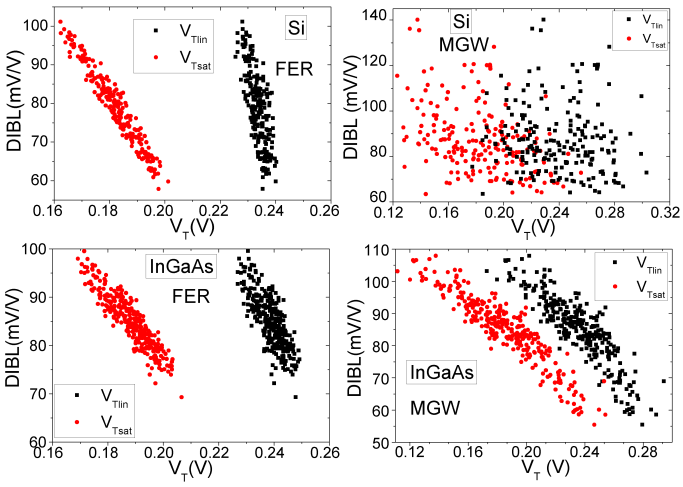

Fig. 6. Scatter plots showing the DIBL variation as a function of the V_T, at both low (V_{Dlin}=0.05 V) and high (V_{Dsat}=0.6 V and V_{Dsat}=0.7 V, respectively) drain biases, due to MGW (GS=5 nm) and FER variations (CL=20 nm and RMS=0.6 nm) for the 10.4 nm $In_{0.53}Ga_{0.47}As$ and the 10.7 nm Si FinFETs.

Fig. 6 shows the DIBL variability as a function of V_T at low and high drain biases due to FER (CL=20 nm and RMS=0.6 nm) for the Si (top left figure) and the $In_{0.53}Ga_{0.47}As$ (bottom left figure) FinFETs. For both devices, the DIBL shows strong negative correlations with V_{Tlin} (correlation coefficient (CC) around -0.7) and V_{Tsat} (CC larger than -0.9). In general, the overall narrowing of the channel of the devices due to FER leads to a higher V_T at both low and high drain biases and a better immunity against the short channel effects. We define the threshold voltage shift ($V_{T-shift}$) as the difference between the mean value of statistical sample, $\langle V_T \rangle$ and the threshold voltage for nominal device (see Table II). Thus, the FER-induced $V_{T-shift}$ at both low and high drain biases are around 10 mV for the $In_{0.53}Ga_{0.47}As$ FinFET and increase to around 45 mV for the Si device. The larger DIBL variability observed in the Si FinFET indicates a larger penetration of the electric field into the channel region and therefore a larger loss of gate control at a high drain bias than in the $In_{0.53}Ga_{0.47}As$ device.

C. MGW Impact on FinFET Variability

Fig. 7 shows (from top to bottom) a comparison of the $\log_{10}(I_{OFF})$, SS, DIBL and V_T variability due to MGW for the studied 10.4 nm $In_{0.53}Ga_{0.47}As$ and 10.7 nm Si FinFETs as a function of the drain bias and the average number of grains present in the gate. Note here that we have opted to not represent these magnitudes as a function of the grain size because the results could be misleading since the TiN metal gate area is slightly different for both devices.

The V_T and $\log_{10}(I_{OFF})$ MGWV is very similar for the $In_{0.53}Ga_{0.47}As$ and Si FinFETs when the average number of metal grains in the gate is large (GS small) and slightly smaller for the $In_{0.53}Ga_{0.47}As$ FinFET when the gate is only composed by a few grains. The $In_{0.53}Ga_{0.47}As$ FinFET is noticeably less resilient to the SS MGWV than the Si device. A major transport process affecting the drain current in the sub-threshold region is the S/D tunnelling, which influences the SS. The S/D tunnelling is much larger in the $In_{0.53}Ga_{0.47}As$ device than in the Si counterpart, mostly due to a smaller average effective transport mass, leading to the observed larger variability. However, the variability in the DIBL is smaller for the $In_{0.53}Ga_{0.47}As$ device than that for the Si one because, for this figure of merit, the strength of the quantum carrier confinement becomes the major factor while the impact of the S/D tunnelling decreases at the threshold. The carriers are more weakly confined in the Si device leading to a worse electrostatic integrity and thus to a larger variability.

In the sub-threshold region, the MGWV is the dominant source of V_T and $\log_{10}(I_{OFF})$ fluctuations in both Si and III-V FinFETs when compared to the FER. The FER variability (for a RMS=1 nm) is only comparable to MGWV when the number of grains present in the gate is very large (GS 3 nm). The impact of the MGW and the FER (when CL=20 nm) on the DIBL variability of both devices is similar. However, the FER becomes the largest source of variability affecting the SS of Si FinFETs while, conversely, the MGW is the dominant source influencing the SS of $In_{0.53}Ga_{0.47}As$ FinFETs.

Fig.6 also shows scatter plots of the DIBL variability as a function of V_T at low and high drain biases due to MGWV (GS=5 nm) for the Si (top right figure) and the $In_{0.53}Ga_{0.47}As$ (bottom right figure) FinFETs. For the $In_{0.53}Ga_{0.47}As$ FinFET, the DIBL shows very strong negative correlations with V_T at both low (CC=−0.88) and high drain biases (CC=−0.92). However, for the Si FinFET, the DIBL is practically uncorrelated with V_T at both low (CC is −0.09) and high drain biases (CC=−0.42). The different behaviour observed in the DIBL for both devices can be explained through an analysis of the relation between the threshold voltages at low and high drain biases. Fig. 8 shows the scatter plots of V_{Tlin} versus V_{Tsat} for the Si (left figure) and $In_{0.53}Ga_{0.47}As$ (right figure) FinFETs. The device with an uniform gate has been added for comparative purposes (red line). For the $In_{0.53}Ga_{0.47}As$ FinFET, the threshold voltage at low and high drain biases are very strongly correlated (CC=0.99). On the other hand, for the Si FinFET, the correlation between V_{Tlin} and V_{Tsat} is weaker (CC=0.94). The larger the CC value, the less sensitive the variability is to a change in the drain bias. As previously seen

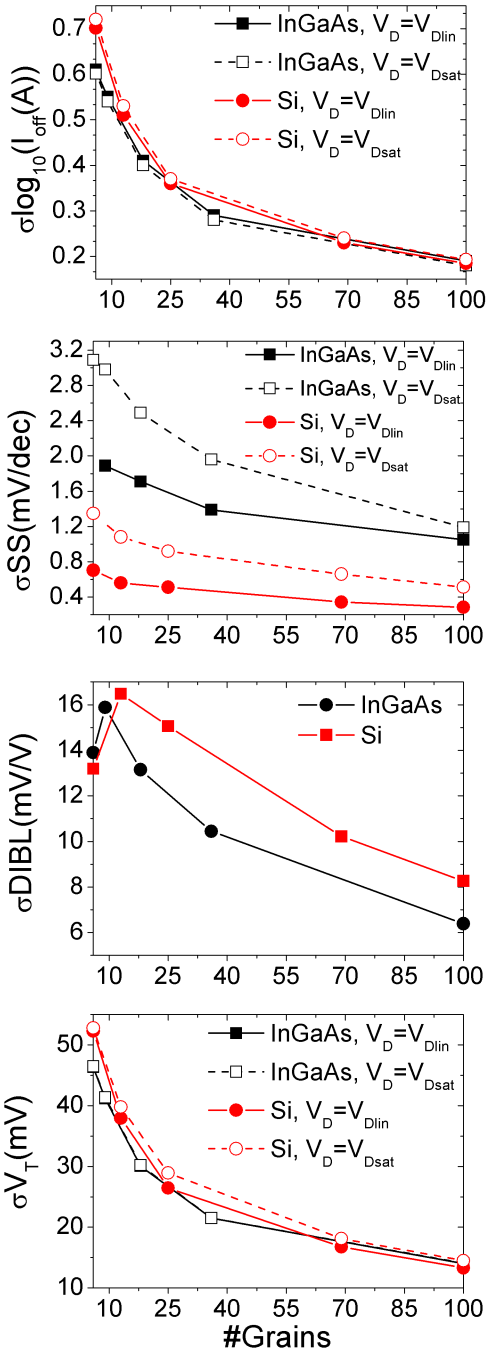

Fig. 7. Comparison of the $\log_{10}(I_{OFF})$, SS, DIBL and V_T variability due to MGW for the studied $In_{0.53}Ga_{0.47}As$ and Si FinFETs as a function of the drain bias (at low V_{Dlin}=0.05 V, at high V_{Dsat}=0.6 V and V_{Dsat}=0.7 V, respectively) and the average number of grains present in the gate.

in Fig. 7, the MGW induced V_T variability is independent of V_D for the $In_{0.53}Ga_{0.47}As$ FinFET whereas, for the Si device, it slightly increases with the applied drain bias.

Fig. 9 shows a comparison of the on-current variability due to MGW for the $In_{0.53}Ga_{0.47}As$ and Si FinFETs as a function of the grain size. As expected, the standard deviation of the I_{ON} decreases with a reduction in the grain size. For the Si FinFET, σI_{ON} ranges from 59 μA/μm when GS=5 nm to 107 μA/μm when GS=10 nm. For the $In_{0.53}Ga_{0.47}As$ FinFET, the on-current variability is around 2.2 times larger than that observed for the Si device, with σI_{ON} ranging from 132 to 237 μA/μm when GS increases from 5 to 10 nm. This

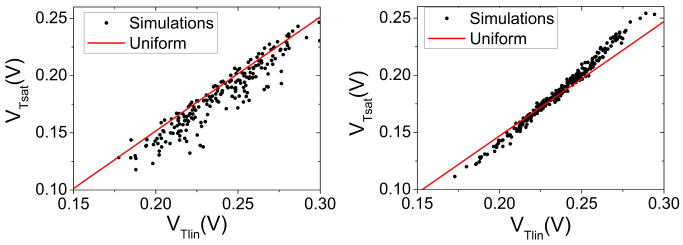

Fig. 8. Scatter plots showing the threshold voltage at a low drain bias (V_{Tlin}) versus the threshold voltage at a high drain bias (V_{Tsat}) due to MGWV for the Si (left) and $In_{0.53}Ga_{0.47}As$ (right) FinFETs. The device with an uniform gate has been added for comparison (red line).

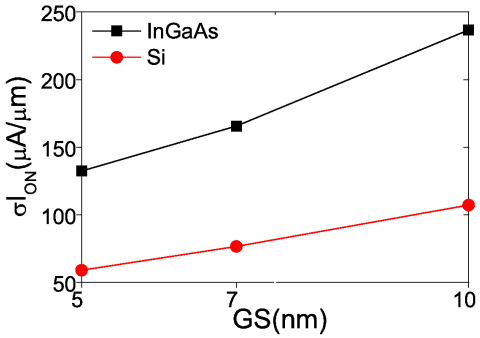

Fig. 9. Comparison of the I_{ON} variability due to MGW for the $In_{0.53}Ga_{0.47}As$ and Si FinFETs as a function of the grain size (GS).

very large on-current variability is related to a lower average electron effective transport mass and thus a higher mobility of III-V materials resulting in a faster carrier transport. The MGWV is recognised as a major source of variability in multi-gate transistors with high-K/metal gate stacks [24], [29] due to much stronger disruptions of electrostatic potential in the channel region controlled by the gate (as compared to the FER or random dopants). The disruptions of electrostatic potential in the $In_{0.53}Ga_{0.47}As$ channel will affect much more its faster non-equilibrium transport thus resulting in a larger difference between the MGWV of the $In_{0.53}Ga_{0.47}As$ and Si devices than that observed for the FER variability. For the Si FinFET, the impact of the FER and MGW variabilities on the on-current is similar. However, for the $In_{0.53}Ga_{0.47}As$ FinFET, the MGW and FER induced on-current standard deviations are only similar when GS=5 nm and RMS=1.0 nm. Any other combination of parameters will lead to a larger MGWV than the variability observed due to the FER.

IV. Conclusion

A 3-D quantum-corrected FE DD and MC simulation study of two sources of statistical variability induced by the fin-edge roughness (FER) and the metal gate work-function (MGW) is performed for the $In_{0.53}Ga_{0.47}As$ with a gate length of 10.4 nm and Si FinFET with a gate length of 10.7 nm. We have analysed the influence of these two sources of variability on five figures of merit: 1) threshold voltage, 2) sub-threshold slope, 3) off-current, 4) drain-induced-barrier-lowering and 5) on-current. This study is done at both low (0.05 V) and high drain biases (0.6 V for the $In_{0.53}Ga_{0.47}As$ FinFET and 0.7 V for the Si device). The main conclusions can be summarised as follows; in the sub-threshold region:

- The V_T and $\log_{10}(I_{OFF})$ MGWV is very similar for the InGaAs and Si FinFETs when the GS is small, and slightly smaller for the InGaAs FinFET when the GS is large.
- The InGaAs FinFET is less resilient to the SS MGWV than the Si device but there is a smaller variability in the DIBL for the InGaAs device than that for the Si counterpart because of a stronger quantum electron confinement in the III-V channel.
- In the presence of FER, the V_T, $\log_{10}(I_{OFF})$, SS and DIBL variations in the InGaAs FinFET are generally smaller at both low and high drain biases than the ones observed in the Si FinFET.
- The MGW variability is the dominant source of V_T and $\log_{10}(I_{OFF})$ fluctuations in both Si and III-V FinFETs when compared to the FER.

In the on-region:

- The on-current variability due to FER is between 1.1-1.5 times larger for the InGaAs FinFET than for the Si device.
- The on-current variability due to MGW is around 2.2 times larger for the InGaAs FinFET than for the Si device.
- For the Si FinFET, the impact of the FER and MGW variabilities on the on-current is similar.
- For the InGaAs FinFET, the on-current MGW variability is generally larger than that observed due to the FER.

References

[1] T. B. Hook, "Fully depleted devices for designers: FDSOI and FinFETs", in Proc. Custom Integrated Circuits Conf., pp. 1-7, 2012

[2] K. Kalna, N. Seoane, A. J. Garcia-Loureiro, I. G. Thayne, and A. Asenov, "Benchmarking of scaled InGaAs implant free NanoMOSFETs", *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2297-2306, 2008.

[3] G. Zheng, A. Carlson, L.T. Pang, K.T. Duong, T.J. King Liu and B. Nikolic, "Large-scale SRAM variability characterisation in 45 nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 3174-3192, 2009.

[4] Y. Cao, J. Velamala, K. Sutaria, M.S. Chen, J. Ahlbin, I. Sanchez Esqueda, M. Bajura, M. Fritze, "Cross-Layer Modeling and Simulation of Circuit Reliability", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no.1, pp. 8-23, 2014.

[5] C. Zhuo, K. Chopra, D. Sylvester and D. Blaauw, "Process Variation and Temperature-Aware Full Chip Oxide Breakdown Reliability Analysis", *IEEE Trans. on Computer-Aided Design*, vol. 30, no. 9, pp. 1321-1333, 2011.

[6] N. Seoane, G. Indalecio, E. Comesana, M. Aldegunde, A. J. Garcia-Loureiro, and K. Kalna, "Random Dopant, Line-Edge Roughness, and Gate Workfunction Variability in a Nano InGaAs FinFET", *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 466–472, 2014.

[7] G. Leung and C. O. Chui, "Variability of inversion-mode and junctionless FinFETs due to line edge roughness", *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1489-1491, 2011.

[8] N. Agrawal, Y. Kimura, R. Arghavani and S. Datta, "Impact of transistor architecture (bulk planar, trigate on bulk, ultrathin-body planar SOI) and material (silicon or III-V semiconductor) on variation for logic and SRAM applications", *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3298-3304, 2013.

[9] International Technology Roadmap for Semiconductors (ITRS), 2013 Edition, http://www.itrs.net/Links/2013ITRS/Summary2013.htm

[10] M. Aldegunde, A. J. García-Loureiro, and K. Kalna, "3D Finite Element Monte Carlo Simulations of Multigate Nanoscale Transistors", *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1561-1567, 2013.

[11] N. Seoane, M. Aldegunde, A. J. Garcia-Loureiro, R. Valin, and K. Kalna, "3D 'atomistic' simulations of dopant induced variability in nanoscale implant free $In_{0.75}Ga_{0.25}As$ MOSFETs", *Solid-St. Electron.*, vol. 69, pp. 43-49, 2012.

[12] N. Seoane, G. Indalecio, E. Comesaña, A. J. García-Loureiro, M. Aldegunde and K. Kalna, "Three-dimensional simulations of random dopant and metal-gate workfunction variability in an $In_{0.53}Ga_{0.47}As$ GAA MOSFET", *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 205-207, 2013.

[13] A. J. Garcia-Loureiro, N. Seoane, M. Aldegunde, R. Valin, A. Asenov, A. Martinez and K. Kalna, "Implementation of the density gradient quantum corrections for 3D simulations of multigate nanoscaled transistors", *IEEE Trans. Comput-Aided Des. Integr. Circuits Syst.*, vol. 30, no. 6, pp. 841-851, 2011.

[14] A. Islam and K. Kalna, "Monte Carlo simulations of mobility in doped GaAs using self-consistent Fermi-Dirac statistics", *Semicond. Sci. Technol.*, vol. 26, No. 5, 055007 (9pp), 2011.

[15] ATLAS Users Manual, Silvaco Inc., pp. 13-1-24, 2012.

[16] A. Martinez, M. Aldegunde, N. Seoane, A.R. Brown and A. Asenov, "Quantum-Transport Study on the Impact of Channel Length and Cross Sections on Variability Induced by Random Discrete Dopants in Narrow Gate-All-Around Silicon Nanowire Transistors",*IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2209-2217, 2011.

[17] J. Lindberg, M. Aldegunde, D. Nagy, W.G. Dettmer, K. Kalna, A.J. Garcia-Loureiro and D. Peric, "Quantum Corrections Based on the 2-D Schrödinger Equation for 3-D Finite Element Monte Carlo Simulations of Nanoscaled FinFETs", *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 423-429, 2014.

[18] C. Jacoboni and P. Lugli, *The Monte Carlo Method for Semiconductor Device Simulation*. New York, Springer-Verlag, 1989.

[19] D. K. Ferry, *Semiconductor Transport*. NY, Taylor & Francis, 2000.

[20] B. K. Ridley, "Reconciliation of the Conwell-Weisskopf and Brooks-Herring formulae for charged-impurity scattering in semiconductors: Third-body interference", *J. Phys. C, Solid State Phys.*, vol.10, no.10, pp.1589-1593, 1977.

[21] A. Islam, B. Benbakhti, and K. Kalna, "Monte Carlo study of ultimate channel scaling in Si and $In_{0.3}Ga_{0.7}As$ bulk MOSFETs", *IEEE Trans. Nanotechnol.*, vol.10, no.6, pp.1424-1432, 2011.

[22] Y. Liu, N. Neophytou, G. Klimeck and M. S. Lundstrom, "Band-Structure Effects on the Performance of IIIV Ultrathin-Body SOI MOSFETs", *IEEE Trans. Electron Devices*, vol. 55, no. 5, pp. 1116-1122, 2008.

[23] A. Asenov, S. Kaya and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness", *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1254-1259, 2003.

[24] G. Indalecio, M. Aldegunde, N. Seoane, K. Kalna and A. J. Garcia-Loureiro, "Statistical study of the influence of LER and MGG in SOI MOSFET", *Semicond. Sci. Technol.*, vol.29, pp. 045005 (7pp), 2014.

[25] X. Wang, A. R. Brown, B. Cheng and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs", *IEDM Tech. Dig.*, pp. 103-106, 2011.

[26] D. Reid, C. Millar, S. Roy and A. Asenov, "Understanding LER-Induced MOSFET Vt variability", *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 2801-2807, 2010.

[27] M. G. Ancona and G. J. Iafrate, "Quantum correction to the equation of state of an electron gas in a semiconductor", *Phys. Rev. B*, vol. 39, no. 13, pp. 9536-9540, 1989.

[28] M. G. Ancona, "Density-gradient theory: a macroscopic approach to quantum confinement and tunneling in semiconductor devices", *J. Comput. Electron.*, vol. 10, pp. 65-97, 2011.

[29] H. F. Dadgour, K. Endo, V. K. De, and K. Banerjee, "Grain- orientation induced work function variation in nanoscale metal-gate transistors–Part I: Modeling, analysis, and experimental validation", *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2504–2514, Oct. 2010.

[30] J. J. Gu, H. Wu, Y. Liu, A. T. Neal, R. G. Gordon and P. D. Ye, "Size-Dependent Transport Study of $In_{0.53}Ga_{0.47}As$ Gate-All-Around Nanowire MOSFETs: Impact of Quantum Confinement and Volume Inversion", *IEEE Electron Device Letters*, vol. 33, no. 7, pp. 967–969, 2012.